1、General Description

The 74HC/HCT125 is a quad buffer/line driver with 3-state outputs controlled by the output enable inputs ($n\overline{OE}$). A HIGH on $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features:

- Input levels:
  For 74HC125: CMOS level
  For 74HCT125: TTL level
- Specified from -40℃ to +85℃
- Packaging information: DIP14/SOP14/TSSOP14

2、Block Diagram And Pin Description

2.1、Block Diagram

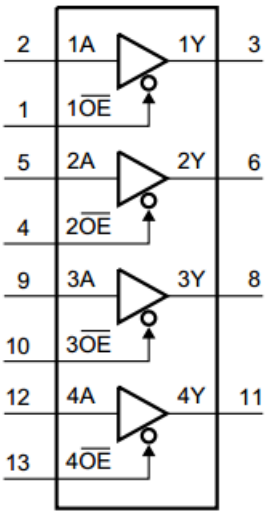


Figure 1. Logic symbol

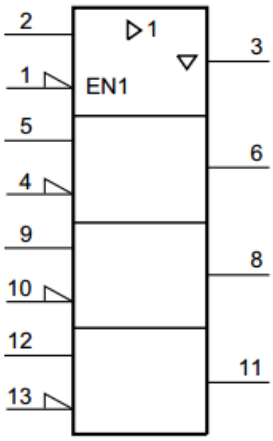


Figure 2. IEC logic symbol

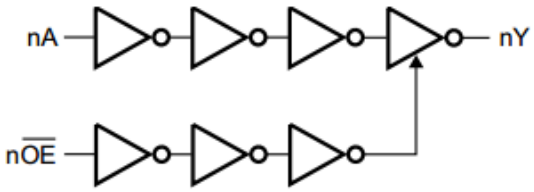
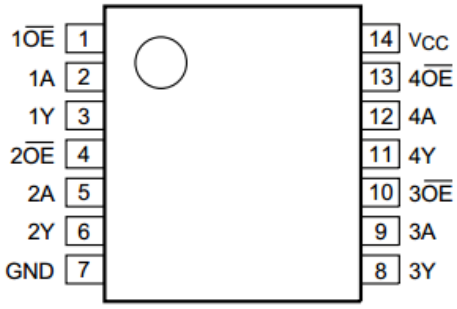


Figure 3. Logic diagram for one gate

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	1$\overline{OE}$	output enable input (active LOW)
2	1A	data input
3	1Y	data output
4	2$\overline{OE}$	output enable input (active LOW)
5	2A	data input
6	2Y	data output
7	GND	ground (0V)
8	3Y	data output
9	3A	data input
10	3$\overline{OE}$	output enable input (active LOW)
11	4Y	data output
12	4A	data input
13	4$\overline{OE}$	output enable input (active LOW)
14	V_{CC}	supply voltage

2.4、Function Table

Control	Input	Output
n$\overline{OE}$	**nA**	**nY**
L	L	L
L	H	H
H	X	Z

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7	V
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
output current	I_O	-0.5V < V_O < V_{CC}+0.5V		-	±35	mA
supply current	I_{CC}	-		-	70	mA
ground current	I_{GND}	-		-70	-	mA
total power dissipation	P_{tot}	-		-	500	mW
storage temperature	T_{stg}	-		-65	+150	℃
Soldering temperature	T_L	10s	DIP	245		℃
			SOP	250		

Note:

[1] For DIP14 packages: above 70℃ the value of P_{tot} derates linearly with 12mW/K.

[2] For SOP14 packages: above 70℃ the value of P_{tot} derates linearly with 8mW/K.

[3] For (T)SSOP14 packages: above 60℃ the value of P_{tot} derates linearly with 5.5mW/K.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
74HC125						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+85	℃
74HCT125						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	-	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	-	ns/V
ambient temperature	T_{amb}	-	-40	-	+85	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC125							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-7.8mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=7.8mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I= V_{CC} or GND; V_{CC}=6.0V		-	-	±0.1	uA
OFF-state output current	I_{OZ}	V_I = V_{IH} or V_{IL}; V_O= V_{CC} or GND; V_{CC}=6.0V		-	-	±0.5	uA
supply current	I_{CC}	V_I= V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
input capacitance	C_I	-		-	3.5	-	pF
74HCT125							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	1.6	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.98	4.32	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	0.16	0.26	V
input leakage current	I_I	V_I= V_{CC} or GND; V_{CC}=5.5V		-	-	±0.1	uA
OFF-state output current	I_{OZ}	V_I = V_{IH} or V_{IL}; V_O= V_{CC} or GND; V_{CC}=5.5V		-	-	±0.5	uA
supply current	I_{CC}	V_I= V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	8.0	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; I_O=0A; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V		-	100	360	uA
input capacitance	C_I	-		-	3.5	-	pF

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC125							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-7.8mA; V_{CC}=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=7.8mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I= V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
OFF-state output current	I_{OZ}	V_I = V_{IH} or V_{IL}; V_O= V_{CC} or GND; V_{CC}=6.0V		-	-	±5	uA
supply current	I_{CC}	V_I= V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
input capacitance	C_I	-		-	-	-	pF
74HCT125							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.84	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	-	0.33	V
input leakage current	I_I	V_I= V_{CC} or GND; V_{CC}=5.5V		-	-	±1	uA
OFF-state output current	I_{OZ}	V_I = V_{IH} or V_{IL}; V_O= V_{CC} or GND; V_{CC}=5.5V		-	-	±5	uA
supply current	I_{CC}	V_I= V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; I_O=0A; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V		-	-	450	uA
input capacitance	C_I	-		-	-	-	pF

3.3.3、AC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC125							
nA to nY propagation delay	t_{pd}	see Figure 5	V_{CC}=2.0V	-	30	100	ns
			V_{CC}=4.5V	-	11	20	ns
			V_{CC}=5.0V;C_L=15pF	-	9	-	ns
			V_{CC}=6.0V	-	9	17	ns
$\overline{nOE}$ to nY enable time	t_{en}	see Figure 6	V_{CC}=2.0V	-	41	125	ns
			V_{CC}=4.5V	-	15	25	ns
			V_{CC}=6.0V	-	12	21	ns
$\overline{nOE}$ to nY disable time	t_{dis}	see Figure 6	V_{CC}=2.0V	-	41	125	ns
			V_{CC}=4.5V	-	15	25	ns
			V_{CC}=6.0V	-	12	21	ns
transition time	t_t	see Figure 5	V_{CC}=2.0V	-	14	60	ns
			V_{CC}=4.5V	-	5	12	ns
			V_{CC}=6.0V	-	4	10	ns
power dissipation capacitance	C_{PD}	C_L=50pF;f=1MHz; V_I =GND to V_{CC}		-	22	-	pF
74HCT125							
nA to nY propagation delay	t_{pd}	see Figure 5	V_{CC}=4.5V	-	15	25	ns
			V_{CC}=5.0V;C_L=15pF	-	12	-	ns
$\overline{nOE}$ to nY enable time	t_{en}	see Figure 6	V_{CC}=4.5V	-	15	28	ns
$\overline{nOE}$ to nY disable time	t_{dis}	see Figure 6	V_{CC}=4.5V	-	15	25	ns
transition time	t_t	see Figure 5	V_{CC}=4.5V	-	5	12	ns
power dissipation capacitance	C_{PD}	C_L=50pF;f=1MHz; V_I =GND to V_{CC}-1.5V		-	24	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_{en} is the same as t_{PZL} and t_{PZH}.

[3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[4] t_t is the same as t_{THL} and t_{TLH}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=(C_{PD}\times V_{CC}^2\times f_i\times N)+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC125							
nA to nY propagation delay	t_{pd}	see Figure 5	V_{CC}=2.0V	-	-	125	ns
			V_{CC}=4.5V	-	-	25	ns
			V_{CC}=5.0V;C_L=15pF	-	-	-	ns
			V_{CC}=6.0V	-	-	21	ns
$n\overline{OE}$ to nY enable time	t_{en}	see Figure 6	V_{CC}=2.0V	-	-	155	ns
			V_{CC}=4.5V	-	-	31	ns
			V_{CC}=6.0V	-	-	26	ns
$n\overline{OE}$ to nY disable time	t_{dis}	see Figure 6	V_{CC}=2.0V	-	-	155	ns
			V_{CC}=4.5V	-	-	31	ns
			V_{CC}=6.0V	-	-	26	ns
transition time	t_t	see Figure 5	V_{CC}=2.0V	-	-	75	ns
			V_{CC}=4.5V	-	-	15	ns
			V_{CC}=6.0V	-	-	13	ns
power dissipation capacitance	C_{PD}	C_L=50pF;f=1MHz; V_I =GND to V_{CC}		-	-	-	pF
74HCT125							
nA to nY propagation delay	t_{pd}	see Figure 5	V_{CC}=4.5V	-	-	31	ns
			V_{CC}=5.0V;C_L=15pF	-	-	-	ns
$n\overline{OE}$ to nY enable time	t_{en}	see Figure 6	V_{CC}=4.5V	-	-	35	ns
$n\overline{OE}$ to nY disable time	t_{dis}	see Figure 6	V_{CC}=4.5V	-	-	31	ns
transition time	t_t	see Figure 5	V_{CC}=4.5V	-	-	15	ns
power dissipation capacitance	C_{PD}	C_L=50pF;f=1MHz; V_I =GND to V_{CC}-1.5V		-	-	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_{en} is the same as t_{PZL} and t_{PZH}.

[3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[4] t_t is the same as t_{THL} and t_{TLH}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=(C_{PD}\times V_{CC}^2\times f_i\times N)+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

4、Testing Circuit

4.1、AC Testing Circuit

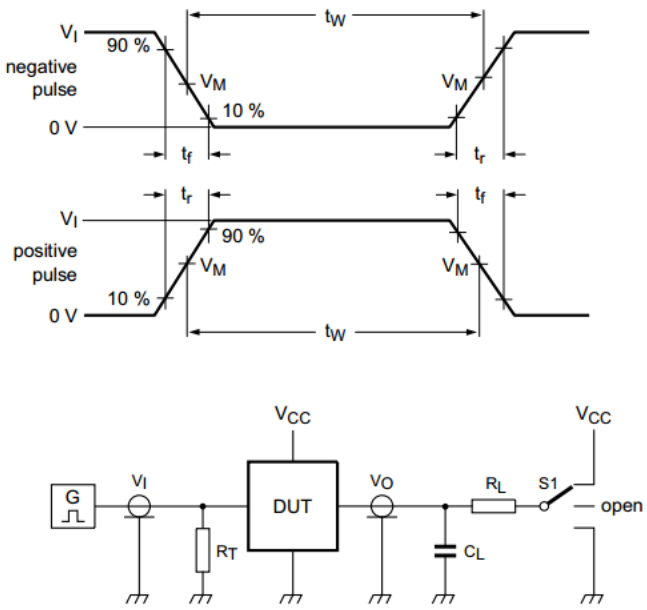


Figure 4. Test circuit for measuring switching times

Definitions for test circuit:

C_L=load capacitance including jig and probe capacitance.

R_T=termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L= Load resistance.

S1 = Test selection switch.

4.2、AC Testing Waveforms

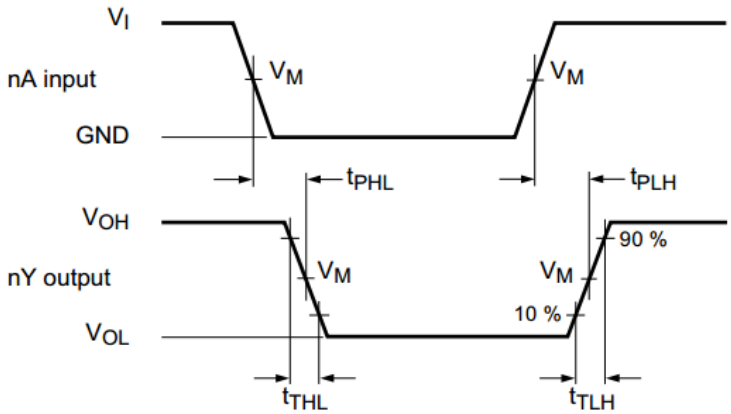


Figure 5. Propagation delay input (nA) to output (nY)

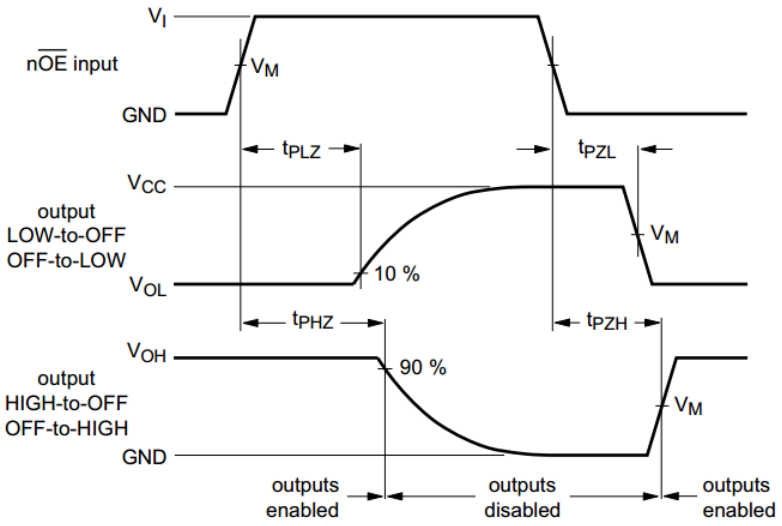


Figure 6. Enable and disable times

4.3、Measurement Points

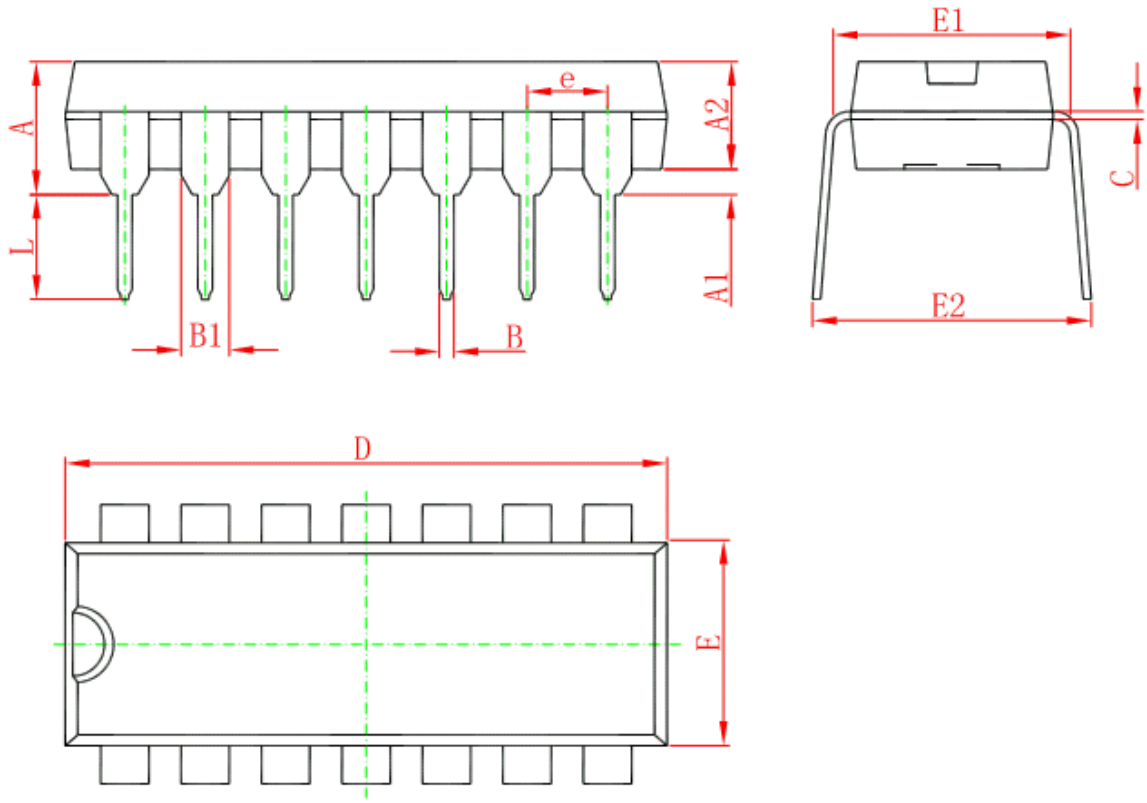
Type	Input	Output
	V_M	V_M
74HC125	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT125	1.3V	1.3V

4.4、Test Data

Type	Input		Load		S1 position		
	V_I	t_r , t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC125	V_{CC}	6.0ns	15pF, 50pF	1kΩ	open	GND	V_{CC}
74HCT125	3V	6.0ns	15pF, 50pF	1kΩ	open	GND	V_{CC}

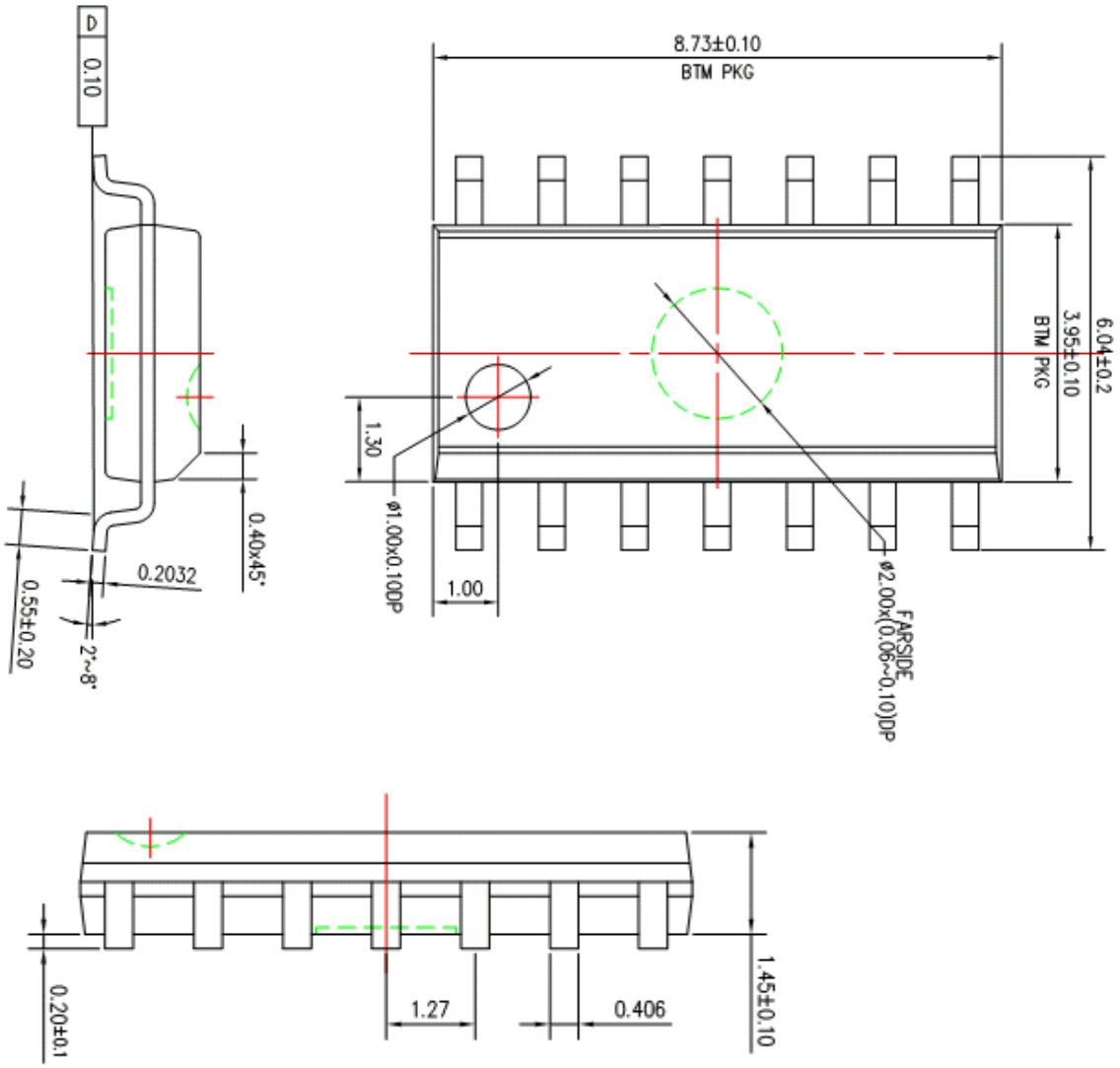
5、Package Information

5.1、DIP14

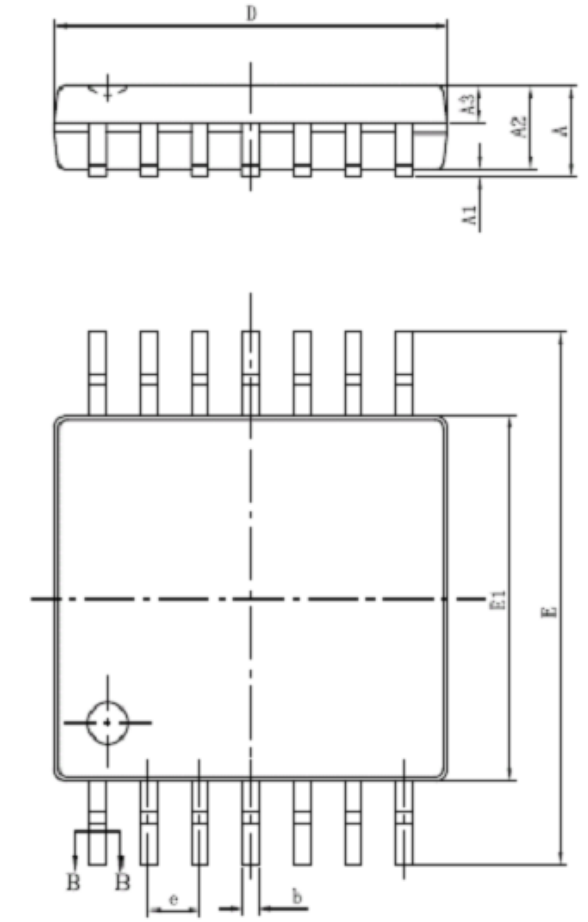


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

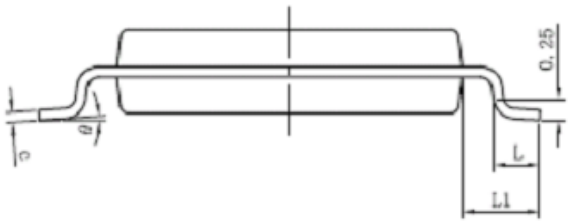
5.2、SOP14

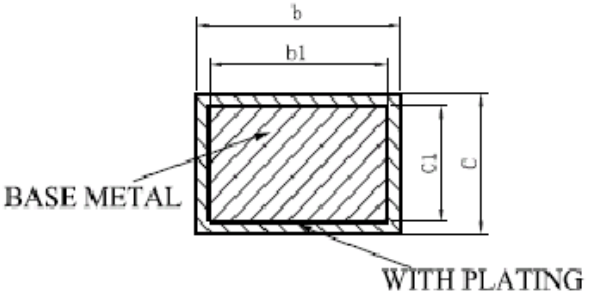

0.10
8.73±0.10
BTM PKG
6.04±0.2
3.95±0.10
BTM PKG
1.30
Ø1.00x0.100P
1.00
Ø2.00x(0.06~0.10)DP
FARSIDE
0.40x45°
0.2032
0.55±0.20
2°~8°
0.20±0.1
1.27
0.406
1.45±0.10

5.3、TSSOP14



SYMBOL	MILLIMETER	
	MIN	MAX
A	—	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.39	0.49
b	0.20	0.30
b1	0.19	0.25
c	0.13	0.19
c1	0.12	0.14
D	4.86	5.06
E1	4.30	4.50
E	6.20	6.60
e	0.65BSC	
L	0.45	0.75
L1	1.00BSC	
θ	0	8°





SECTION B-B

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard。 ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements。									

6.2、Notion

Recommended carefully reading this information before the use of this product；

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