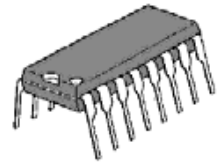
General Description

The KA3525-100 is a monolithic integrated circuit that includes all of the control circuits necessary for a pulse width modulating regulator. There are a voltage reference, an error amplifier, a pulse width modulator, an oscillator, an under voltage lockout, a soft start circuit, and the output driver in the chip.

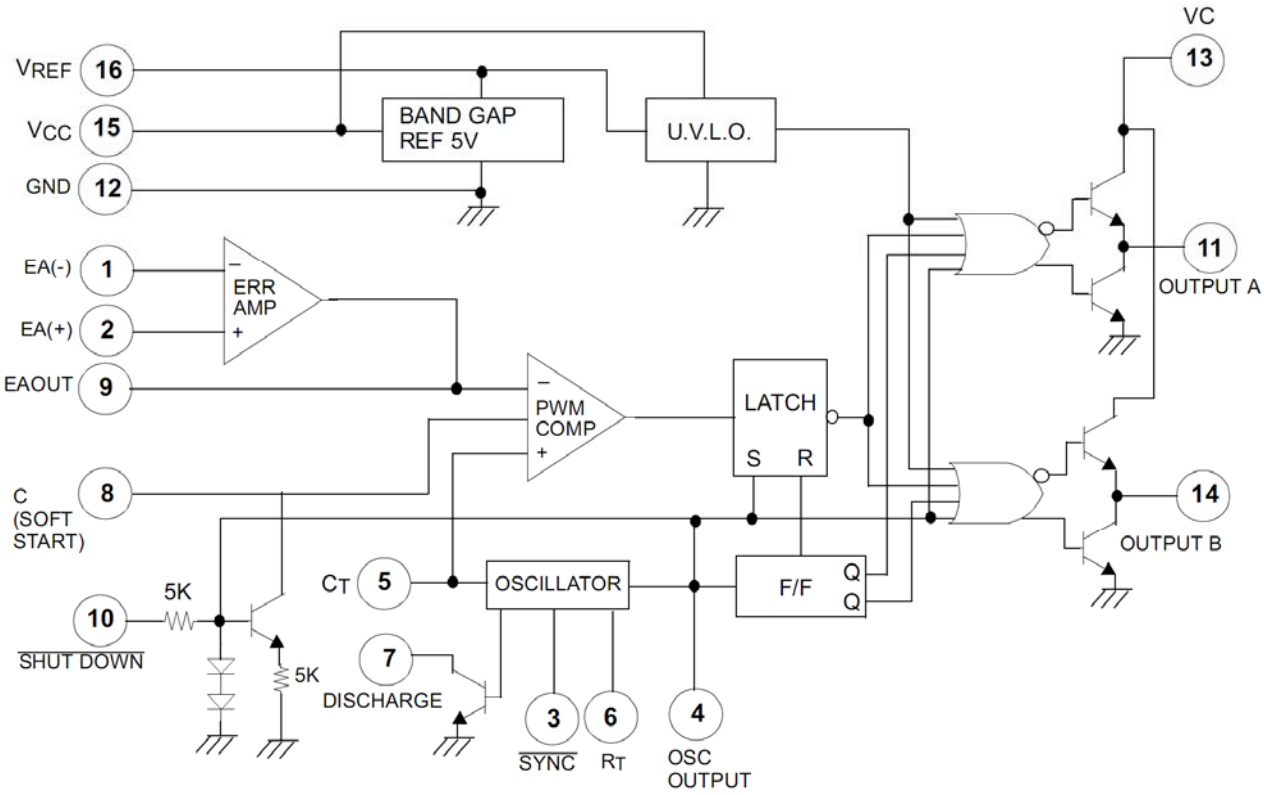

DIP16

KA3525-100 is available in DIP16 package.

Features

- 5V ±1% Reference
- Oscillator Sync Terminal
- Internal Soft Start
- Dead Time Control
- Under Voltage Lockout

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	40	V
Collector Supply Voltage	V_C	40	V
Output Current, Sink or Source	I_O	500	mA
Reference Output Current	I_{REF}	50	mA
Oscillator Charging Current	$I_{CHG(OSC)}$	5	mA
Power Dissipation (T_A=25℃)	P_D	1000	m/W
Operating Temperature	T_{OPR}	0～+70	℃
Storage Temperature	T_{STG}	-65～+150	℃
Lead Temperature (Soldering, 10sec)	T_{LEAD}	+300	℃

Electrical Characteristics

(V_{CC}= 20V, T_A =0 to 70°C , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
REFERENCE SECTION						
Reference Output Voltage	V_{REF}	T_J =25°C	5.0	5.1	5.2	V
Line Regulation	ΔV_{REF}	V_{CC}= 8 to 35V		9	20	mV
Load Regulation	ΔV_{REF}	I_{REF}=0 to 20mA		20	50	mV
Short Circuit Output Current	I_{SC}	V_{REF}=0, T_J =25°C		80	120	mA
Total Output Variation *1	ΔV_{REF}	Line, Load and Temperature	4.95		5.25	V
Temperature Stability *1	ST_T			20	50	mV
Long Term Stability *1	ST	T_J =125°C, 1KHR$_S$		20	50	mV
OSCILLATOR SECTION						
Initial Accuracy *1,2	ACCUR	T_J =25°C		±3	±6	%
Frequency Change with Voltage	$\Delta f/\Delta V_{CC}$	V_{CC}= 8 to 35V *1,2		±0.8	±2	%
Maximum Frequency	$f_{(MAX)}$	R_T=2kΩ, C_T=470pF	380	430		kHz
Minimum Frequency	$f_{(MIN)}$	R_T=200kΩ, C_T=0.1μF		60	120	Hz
Clock Amplitude *1,2	$V_{(CLK)}$		3	4		V
Clock Width *1,2	$t_{W(CLK)}$	T_J =25°C	0.3	0.6	1	μs
Sync Threshold	$V_{TH(SYNC)}$		1.2	2	2.8	V
Sync Input Current	$I_{I(SYNC)}$	Sync=3.5V		1.3	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM}=5.1V)						
Input Offset Voltage	V_{IO}			1.5	10	mV
Input Bias Current	I_{BIAS}			1	10	μA
Input Offset Current	I_{IO}			0.1	1	μA
Open Loop Voltage Gain	G_{VO}	R_L ≧ 10MΩ	60	80		dB
Common Mode Rejection Ratio	CMRR	V_{CM}=1.5 to 5.2V	60	90		dB
Power Supply Rejection Ratio	PSRR	V_{CC}=8 to 3.5V	50	60		dB

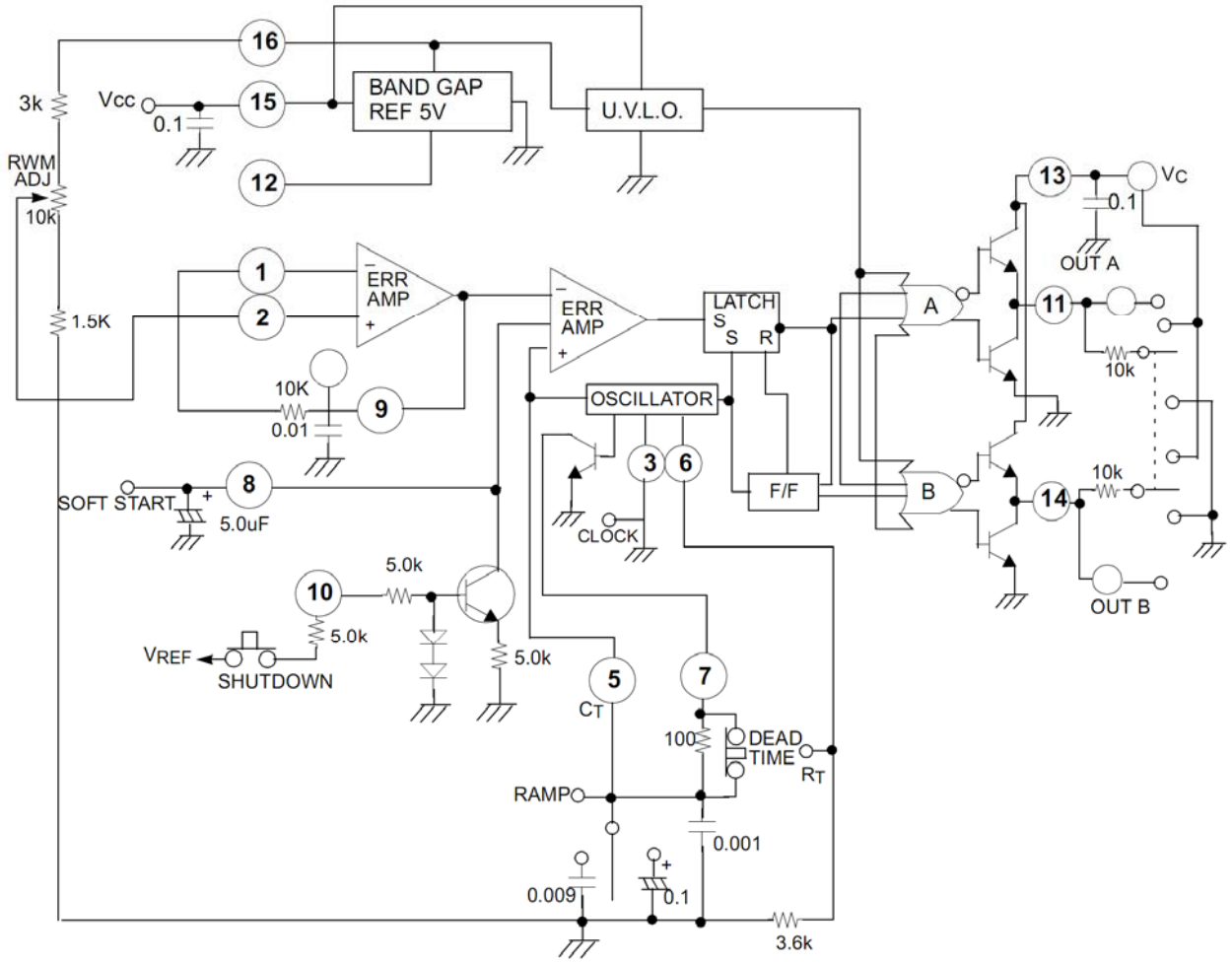
Continued:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM COMPARATOR SECTION						
Minimum Duty Cycle	$D_{(MIN)}$				0	%
Maximum Duty Cycle	$D_{(MAX)}$		45	49		%
Input Threshold Voltage *2	V_{TH1}	Zero Duty Cycle	0.7	0.9		V
Input Threshold Voltage *2	V_{TH2}	Max Duty Cycle		3.2	3.6	V
SOFT-START SECTION						
Soft Start Current	I_{SOFT}	V_{SD}=0V, V_{SS}=0V	25	51	80	μA
Soft Start Low Level Voltage	V_{SL}	V_{SD}=25V		0.3	0.7	V
Shutdown Threshold Voltage	$V_{TH(SD)}$		0.9	1.3	1.7	V
Shutdown Input Current	$I_{N(SD)}$	V_{SD}=2.5V		03	1	mA
OUTPUT SECTION						
Low Output Voltage 1	V_{OL1}	I_{SINK}=20mA		0.1	0.4	V
Low Output Voltage 2	V_{OL2}	I_{SINK}=100mA		0.5	2	V
High Output Voltage 1	V_{CH1}	I_{SOURCE}=20mA	18	19		V
High Output Voltage 2	V_{CH2}	I_{SOURCE}=100mA	17	18		V
Under Voltage Lockout	V_{UV}	V8 and V9=High	6	7	8.5	V
Collector Leakage Current	I_{LKG}	V_{CC}=35V		80	200	μA
Rise Time *1	t_R	C_L=1μF, T_J =25°C		80	600	ns
Fall Time *1	t_F	C_L=1μF, T_J =25°C		70	300	ns
Standby current						
Supply Current	I_{CC}	V_{CC}=35V		12	20	mA

*1. These parameters. although guaranteed over the recommended operating conditions, are not 100% tested in production

*2. Tested at f_{OSC}=40kHz (R_T =3.6K, C_T =0.01uF, R_I = 0Ω)

Test Circuit



Outline Drawing

DIP16 Unit:mm