2269

DATASHEET

Specification Revision History:

Version	Date	Description
V1.0	2020/03	New
V1.1	2021/02	Modify Ordering Information
V1.2	2024/02	Modify Ordering Information
V1.3	2025/01	Add application precautions and overall typesetting.

Description

2269 is a high performance,highly integrated current mode PWM controller for medium to large offline flyback converter applications.
In 2269,the PWM switching is internally trimmed to tight range.To improve EMI performance,the IC integrates frequency shuffling function to reduce conduc- tion EMI emission of a power supply.The IC also integrates Constant Power Limiting block to achieve constant output power limit from 90VAC to 264VAC.
Under light load conditions,a green mode function can continuously decrease the switching frequency.
Under zero-load conditions,the power supply enters into burst mode and provides excellent efficiency without audio noise generated.This green mode function enables power supplies to meet international power conservation requirements.
2269 integrates functions and protections of Under Voltage Lockout (UVLO),VDD Over Voltage Protec- tion (OVP),Soft Start,External Programmable Over Temperature Protection(OTP),Cycle-by-cycle Cur- rent Limiting(OCP),Over Load Protection(OLP), Pins Floating Protection,RI Pin Short-to-GND Protec- tion,GATE Clamping,VDD Clamping,Leading Edge Blanking(LEB).
In 2269,the all protection functions are auto-recovery mode protection.
2269 is available in SOP-8 and DIP-8 packages.

Features

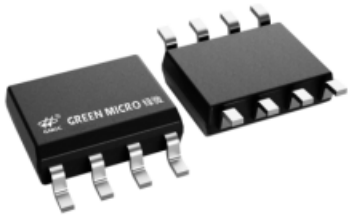
- Built-in Soft Start Function
- Very Low Startup Current
- Frequency Reduction and Burst Mode Control for Energy Saving
- Built-in Frequency Shuffling
- Programmable Switching Frequency
- Built-in Synchronous Slope Compensation
- Cycle-by-Cycle Current Limiting
- Pins Floating Protection
- High Voltage CMOS Process with Excellent ESD Protection
- Current Mode Control
- Built-in Leading Edge Blanking (LEB)
- Constant Power Limiting
- Audio Noise Free Operation
- VDD OVP &Clamp
- VDD Under Voltage Lockout (UVLO)

Applications

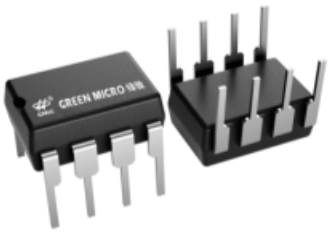
Offline AC/DC Flyback Converter for

- AC/DC Power Adaptors
- Open-frame SMPS
- Print Power,Scanners,and Motor Drivers

The appearance of the product



SOP-8

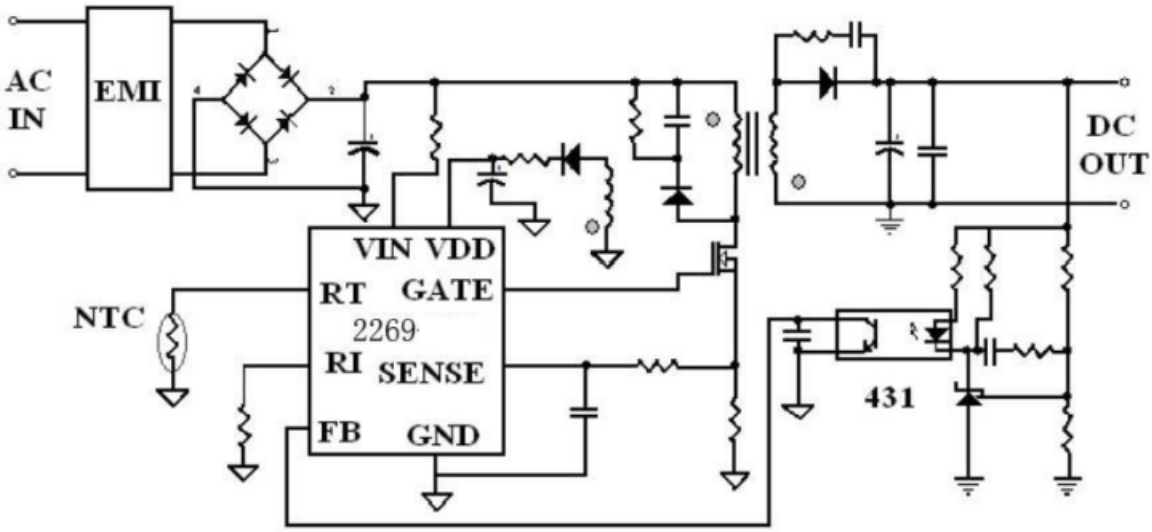


DIP-8

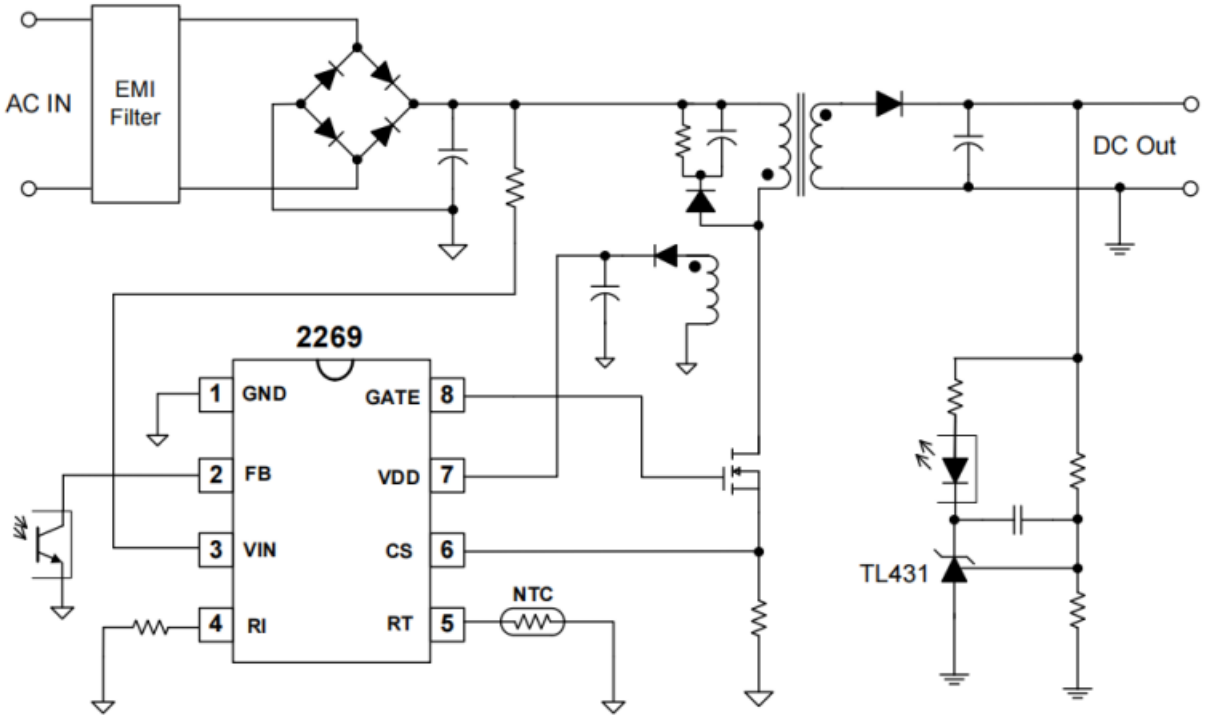
Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
GM2269D	SOP-8	GM2269 245	REEL	2500PCS/REEL
GM2269N	DIP8	GM2269 245	TUBE	2000PCS/BOX
2269(GMIC)	SOP-8	GM2269 45	REEL	2500PCS/REEL
2269(GMIC)	DIP8	GM2269 GB45	TUBE	2000PCS/BOX

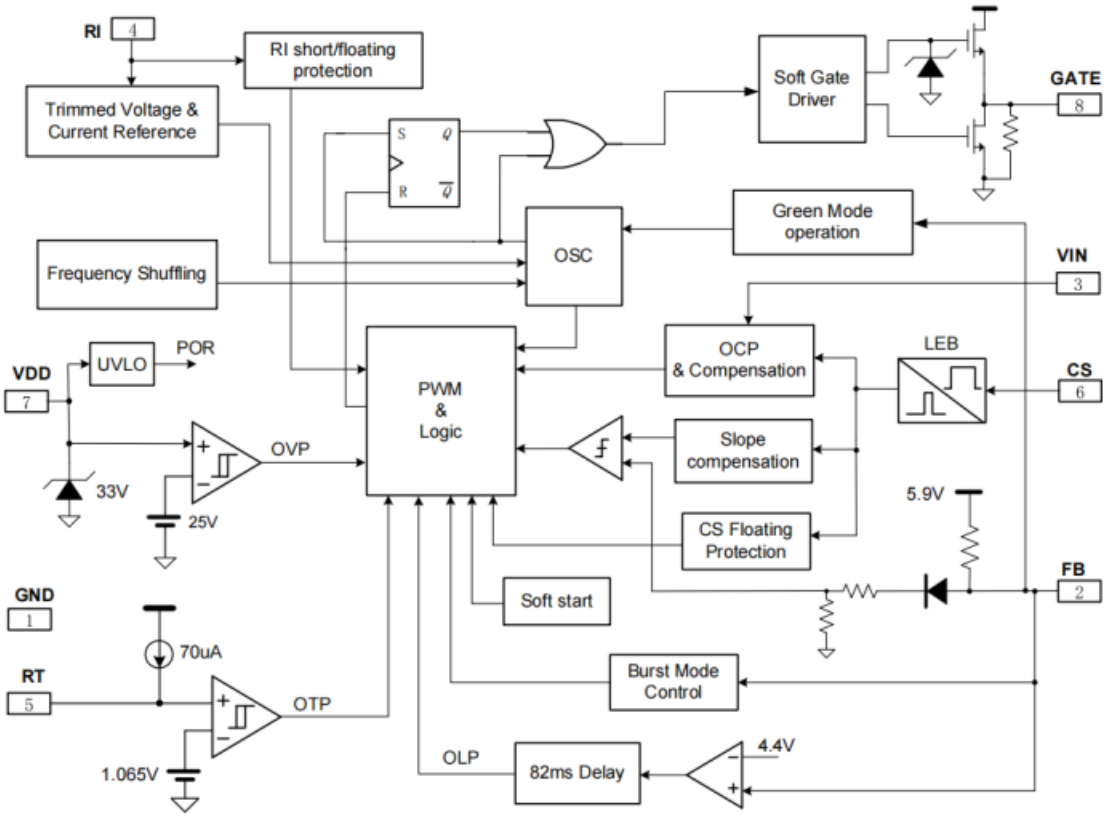
Application Circuit



TYPICAL APPLICATION



Block Diagram



Pin Description

Pin Num	Pin Name	I/O	Description
1	GND	P	IC ground pin.
2	FB	1	Voltage feedback pin.The loop regulation is achieved by connecting a photo-coupler to this pin.PWM duty cycle is generated by this pin voltage and the current sense signal at Pin 6.
3	VIN		This pin is connected to the rectified line input via a large value resistor. The function of the pin is for startup and line voltage sensing.
4	RI	I	Set the switching frequency by connecting a resistor between RI and GND.This pin has floating/short-to-GND protection.
5	RT		This pin is for over temperature protection by connecting an external NTC resistor to ground.Once the pin voltage drops below a fixed limit of 1.065V,PWM output will be disabled.
6	CS	II	Current sense input pin.
7	VDD	P	IC power supply pin.
8	GATE	O	Totem-pole gate driver output to drive the external MOSFET.

Absolute Maximum Ratings(Note 1)

Parameter	Value	Unit
VDD/VIN DC Supply Voltage	33	V
VDD DC Clamp Current	10	mA
GATE pin	20	V
FB,RI,RT,CS voltage range	-0.3 to 7	V
Package Thermal Resistance(DIP-8)	90	°CN
Package Thermal Resistance (SOP-8)	150	°CN
Maximum Junction Temperature	150	°C
Operating Temperature Range	-40 to 85	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering,10sec.)	260	°C
ESD Capability,HBM(Human Body Model)	3	kV
ESD Capability,MM(Machine Model)	250	V

Recommended Operation Conditions(Note 2)

Parameter	Value	Unit
Supply Voltage,VDD	11 to 23	V
Operating Frequency	50 to 130	kHz
Operating Ambient Temperature	-40 to 85	°C

ELECTRICAL CHARACTERISTICS

(TA=25°C,Rl=24K ohm,VDD=18V,if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Section(VDD Pin)						
I_Startup	VDD Start up Current	VDD=15V,Measure current into VDD		5	20	uA
I_VDD_Op	Operation Current	V_{FB}=3V,GATE=1nF		2.5	3.5	mA
UVLO(ON)	VDD Under Voltage Lockout Exit(Startup)		15.5	16.5	17.5	V
UVLO(OFF)	VDD Under Voltage Lockout Enter		9.5	10.5	11.5	V
VDD_OVP_ON	VDD Over Voltage Protection trigger		23.5	25	26.5	V
VDD_OVP_Hys	VDD OVP Hysteresis			2		V
VoD_Clamp	VDD Zener Clamp Voltage	I(V_{DD})=5mA		33		V
T_Softstart	System Soft Start Time			3		mSec
Feedback Input Section(FB Pin)						
A_{vcs}	PWM Input Gain	$\triangle V_{FB}/\triangle V_{cs}$		2.8		VN
V_{FB}_Open	FBOpen Voltage			5.9		V
I_{FB}_Short	FB short circuit current	Short FB pin to GND, measure current		1.2		mA
V_{FB}_min_duty	FB under voltage gate clock is off.			1.0		V
V_{TH}_PL	Power Limiting FB Threshold Voltage			4.4		V
T_D_PL	Power limiting Debounce Time	Note 3		82		mSec
Z_{FB}_IN	Input Impedance			5		Kohm
Current Sense Input Section(CS Pin)						
T_blanking	SENSE Input Leading Edge Blanking Time			250		nSec
Vth_OC_max	Internal current limiting threshold	I(VIN)=0	0.85	0.9	0.95	V
T_{p_oc}	Over Current Detection and	GATE=1nF		120		nSec

	Control Delay					
Oscillator Section(RI Pin)						
Fosc	Normal Oscillation		60	65	70	KHZ
	Frequency					
△F(shuffle)/Fosc	Frequency shuffling range	Note 4	-4		4	%
△f_Temp	Frequency Temperature Stability	-40°C to 125°C(Note 4)		5		%
△f_VDD	Frequency Voltage Stability	VDD=12-23V(Note 4)		5		%
Duty_max	Maximum Duty cycle		75	80	85	%
RI range	Operating RI Range		12	24	60	Kohm
V RI open	RI open voltage			2.0		V
F_BM	Burst Mode Base Frequency			22		KHz
Over Temperature Protection(RT Pin)						
I_RT	Output Current of RT Pin			70		uA
VTH_OTP	OTP Threshold Voltage		1.015	1.065	1.115	V
VTH_OTP_OFF	OTP Release Voltage			1.165		V
VTH_OTP_Hys	OTP Hysteresis			0.1		V
V_RT_Open	RT Pin Open Voltage			4.6		V
Gate Drive Output(GATE Pin)						
VOL	Output Low Level	Io=20 mA(sink)			0.3	V
VOH	Output High Level	Io=20 mA(source)	11			V
Gate_Clamp	Output Clamp Voltage Level	VDD=24V		16		V
T r	Output Rising Time	GATE=1nF		120		nSec
T_f	Output Falling Time	GATE=1nF		50		nSec

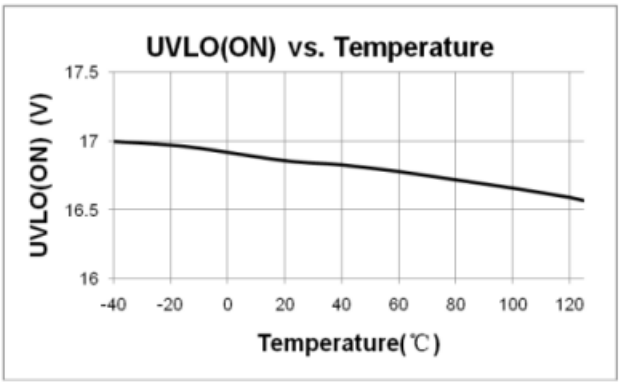
Note 1. Stresses beyond those listed under "Absolute Maximum Ratings"may cause permanent damage to the device.These are stress ratings only,and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

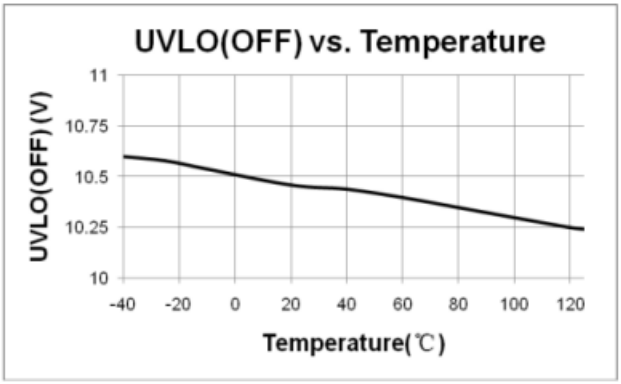
Note 2. The device is not guaranteed to function outside its operating conditions.

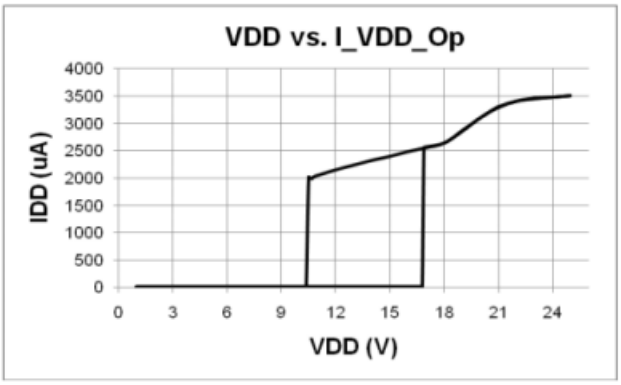
Note 3. The OLP debounce time is proportional to the period of switching cycle.

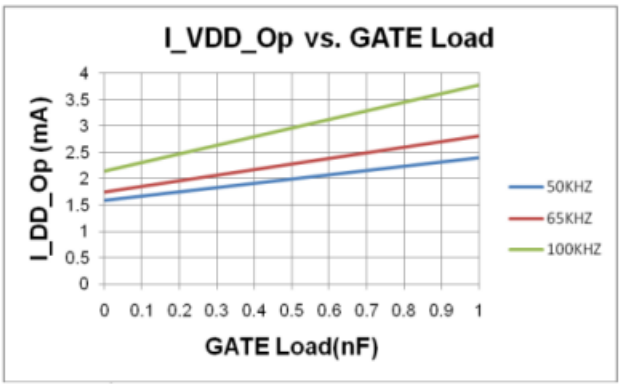
Note 4. Guaranteed by design.

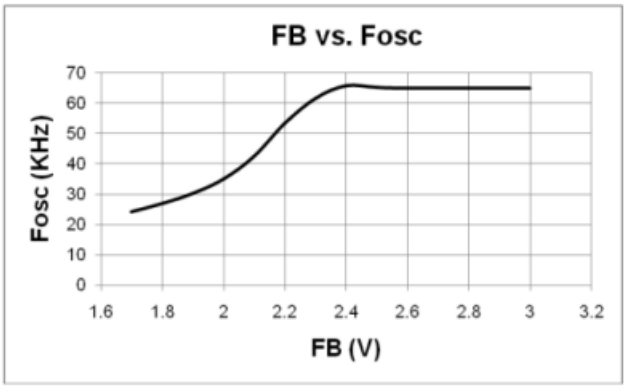
CHARACTERIZATION PLOTS

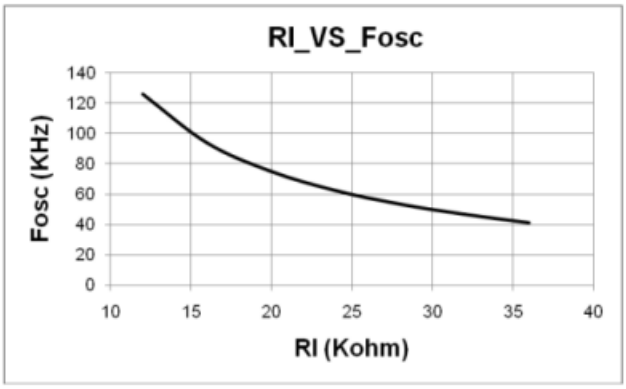


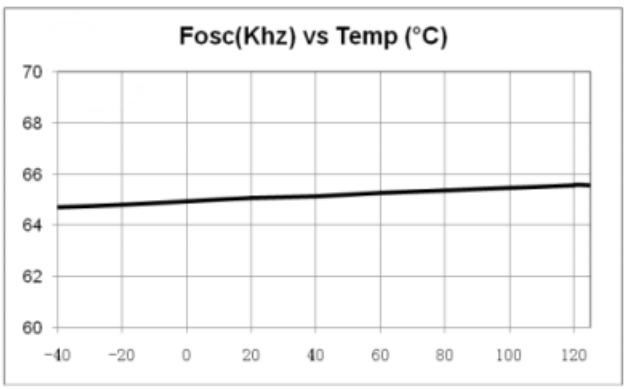


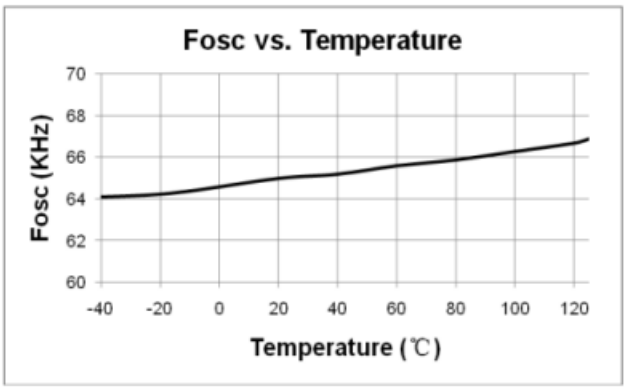


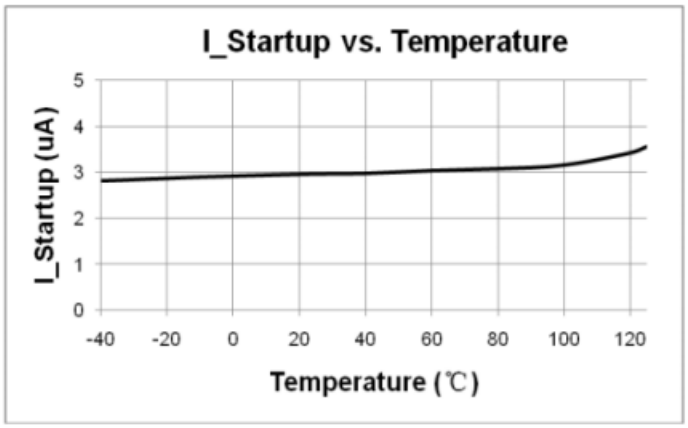


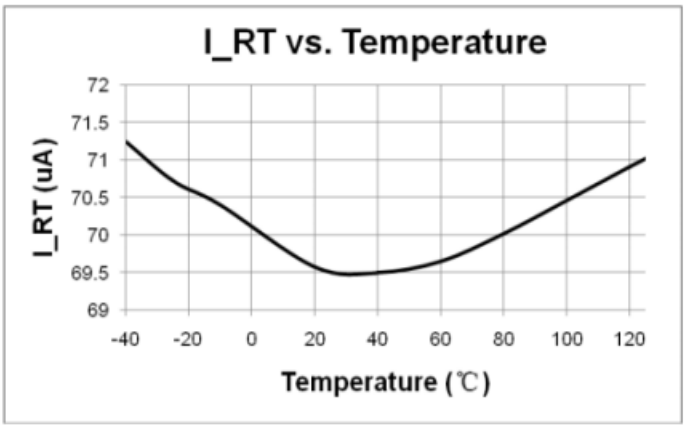


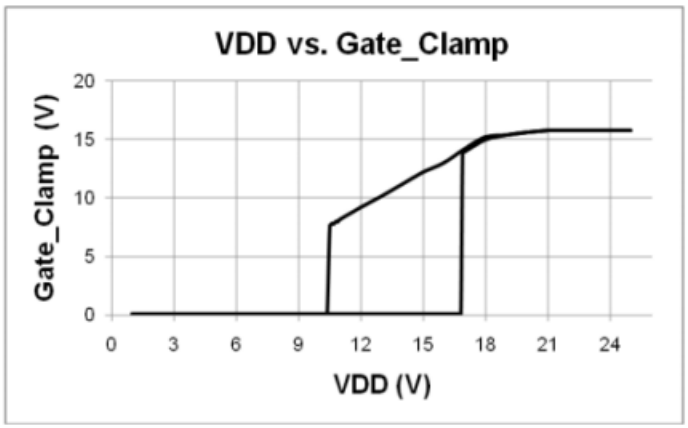


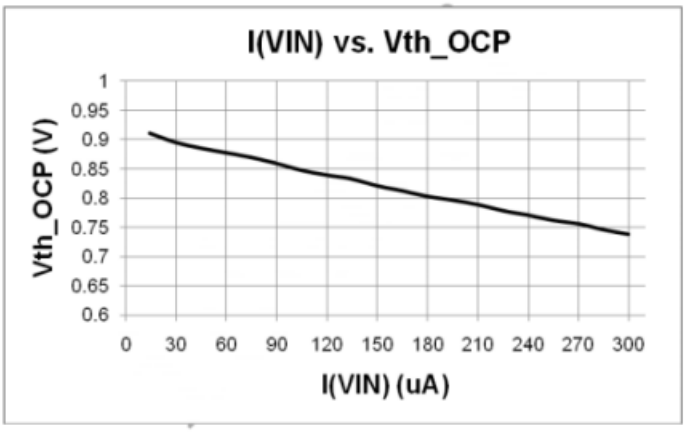





I_Startup vs. Temperature
I_Startup (uA)
5
4
3
2
1
0
-40 -20 0 20 40 60 80 100 120
Temperature (℃)


I_RT vs. Temperature
I_RT (uA)
72
71.5
71
70.5
70
69.5
69
-40 -20 0 20 40 60 80 100 120
Temperature (℃)


VDD vs. Gate_Clamp
Gate_Clamp (V)
20
15
10
5
0
0 3 6 9 12 15 18 21 24
VDD (V)


I(VIN) vs. Vth_OCP
Vth_OCP (V)
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0 30 60 90 120 150 180 210 240 270 300
I(VIN) (uA)

OPERATION DESCRIPTION

2269 is a high performance,highly integrated cur- rent mode PWM controller for medium to large off- line flyback converter applications.The built-in ad- vanced energy saving with high level protection fea- tures improves the SMPS reliability and perfor- mance without increasing the system cost.

◆ Low Startup Current & Operating

Current

The typical startup current of 2269 is only about
5uA so that a high resistance startup resistor can be used to minimize power loss.For an AC/DC adapter with universal input range,a 2M Ohm, 1/8W startup resistor can be used to provide a fast startup and yet low power dissipation design solution.
The operating current in 2269 is as small as 2.3mA(typical).The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

◆ Soft Start

2269 features an internal 3ms (typical)soft start that slowly increases the threshold of cycle-bycycle current limiting comparator during startup se- quence.It helps to prevent transformer saturation and reduce the stress on the secondary diode dur- ing startup.Every restart attempt is followed by a soft start activation.

◆ Oscillator with Frequency Shuffling

Connecting a resistor from RI pin to GND according to the equation below to program the normal switching frequency:

$$F_{osc}(KHz) = \frac{1560}{RI(K\Omega)}$$

It can typically operate between 50kHz to 130kHz. To improve system EMI performance,2269 oper- ates the system with ±4%frequency shuffling around setting frequency.

◆ Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on,a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery.To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period(250ns,typical),the PWM comparator is disabled and cannot switch off the gate driver.Thus,external RC filter with a small time constant is enough for current sensing.

◆ Frequency Reduction for Green Mode

Operation

When the loading is light,the IC will automatically reduce the PWM switching frequency to achieve high efficiency.In the whole frequency reduction process,there is no audio noise generated.

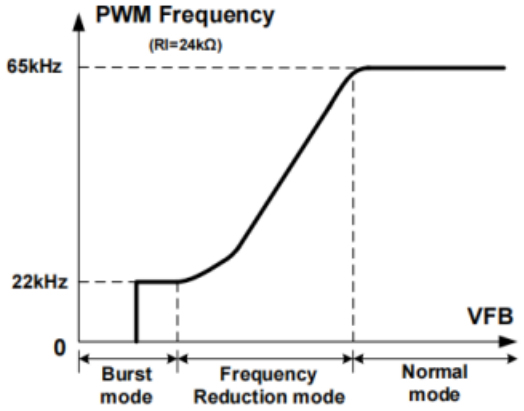


Fig.1

◆ Burst Mode Control

When the loading is very small,the system enters into burst mode.When VFB drops below Vskip, 2269 will stop switching and output voltage starts to drop,which causes the VFB to rise.Once VFB rises above Vskip,switching resumes.Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

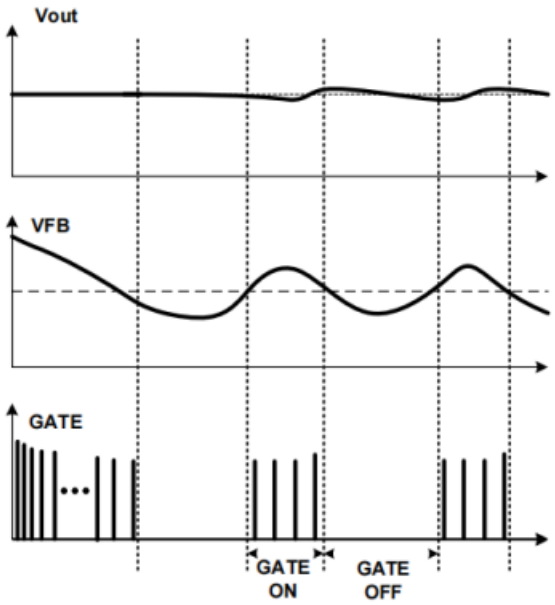


Fig.2

◆ Synchronous Slope Compensation

In the conventional application,the problem of the stability is a critical issue for current mode controlling,when it operates in higher than 50%of the duty-cycle.In 2269,the slope compensation cir- cuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly

improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

◆ Constant Power Limiting

In flyback converter applications,the GATE drive delay can cause system OPP (Over Power Point) to change according to the AC line input voltage.In 2269,an OPP compensation block is integrated to achieve constant max.output power capability over universal AC input range.Since the pin VIN is con- nected to the rectified input line voltage through the startup resistor,the current flowed into the VIN pin indicates the line voltage.Using the information of VIN pin current,the IC adjusts the cycle-by-cycle OCP threshold according to the following equation:

VHLoCp(V)=0.9-0.0278×RI×I(VIN)

In this way,the system OPP variation can be compensated automatically.

◆ Over Temperature Protection

By connecting a NTC resistor in series with a regular resistor between RT and GND,the over temperature protection (OTP)can be realized.NTC resistor value becomes lower when the ambient temperature rises.With the fixed internal current IRT flowing through the resistors,the voltage at RT pin becomes lower at high temperature.The internal OTP comparator is triggered and shut down the PWM signal when the sensed input voltage is lower than the comparator threshold voltage.

OTP is an auto recovery mode protection(as mentioned below).

◆ Auto Recovery Mode Protection

As shown in Fig.3,once a fault condition s detected,switching will stop.This will cause VDD to fall because no power is delivered form the auxiliary winding.When VDD falls to UVLO(off) (typical 10.5V),the protection is reset and the operating current reduces to the startup current, which causes VDD to rise,as shown in Fig.3. However,if the fault still exists,the system will experience the above mentioned process.If the fault has gone,the system resumes normal operation.In this manner,the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

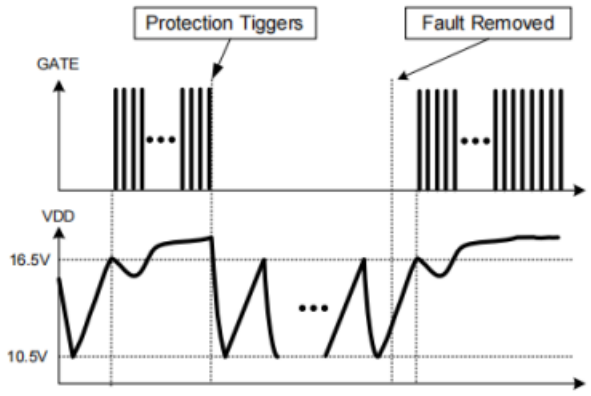


Fig.3

◆ Over Load Protection(OLP)1 Over Current Protection (OCP)/Over Power Protection (OPP) 1 Open Loop Protection(OLP)

When OLP/OCP/OPP/Open Loop occurs,a fault is detected.If this fault is present for more than 82ms (typical),the protection will be triggered,the IC will experience an auto-recovery mode protection as mentioned above,as shown in Fig.4.The 82ms delay time is to prevent the false trigger from the power-on and turn-off transient.

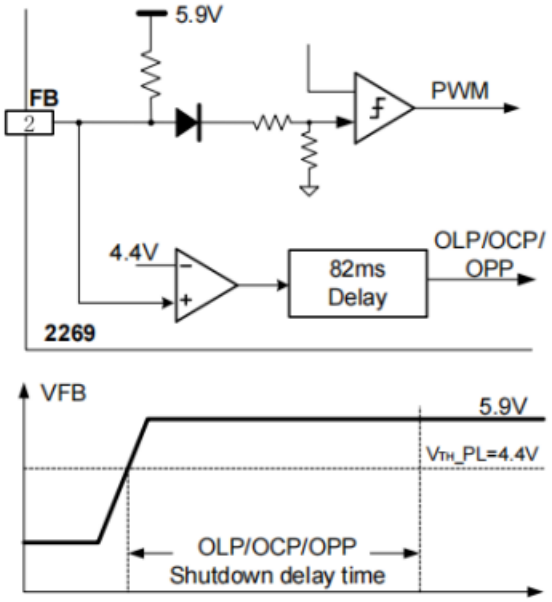


Fig.4

◆ VDD OVP(Over Voltage Protection)

VDD OVP (Over Voltage Protection) is implemented in 2269 and it is a protection of auto recovery mode (as mentioned below).

◆ Pins Floating Protection and RI Pin

Short-to-GND Protection

In 2269,if pin floating situation or RI pin short-to-GND occurs,the protection is triggered immediately and the system will experience the process of auto-recovery mode protection.

◆ Soft Gate Drive

2269 has a fast totem-pole gate driver with 800mA capability.Cross conduction has been avoided to minimize heat dissipation,increase efficiency,and enhance reliability.An internal 16V clamp is added for MOSFET gate protection at higher than expected VDD input.A soft driving waveform is implemented to minimize EMI.

Application Information

The 2269-032 is a highly integrated PWM controller IC optimized for offline flyback con- verter applications.The extended burst mode control greatly reduces the standby power consump- tion and helps the design easily meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of 2269-032 is designed to be very low so that VDD cod be charged up aboveul UVLO(exit)threshold level and device starts up quickly.A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application.For a typical AC/DC adaptor with universal input range design,a 2 MΩ,1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

Operating Current

The Operating current of 2269-032 is low at 2.3mA.Good efficiency is achieved with 2269-032 low operating current together with extended burst mode control schemes.

Frequency shuffling for EMI improvement

The frequency Shuffling/jittering(switching frequency modulation)is implemented in 2269-032.

The oscillation frequency is modulated with a internally generated random source so that the tone energy is evenly spread out.The spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

Burst Mode Operation

At zero load or light load condition,most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET ransistor,the core loss of the transformer and the loss on the snubber circuit.The magnitude of power loss is in proportion to the number of swit- -ching events within a fixed period of time.Reducing switching events leads to the reduction on the power loss and thus conserves the energy.

2269-032 self adjusts the switching mode according to the loading condition.At from no load to light/medium load condition,the FB input drops below burst mode threshold level(1.8V).Device enters Burst Mode control.The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state.Otherwise the gate drive remains at off stateto minimize the switching loss thus reduce the standby power consumption to the greatest xtend.The nature of high frequency switching also reduces the audio noise at any loading conditions.

Oscillator Operation

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined.The relationship between RI and witching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

Fosc=1560/RI(KΩ) (Khz)

Current Sensing and Leading EdgeBlanking

Cycle-by-Cycle current limiting is offered in 2269-032 current mode PWM control.The switch current is detected by a sense resistor into the sense pin.An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recov- ery so that the external RC filtering on sense input is no longer required.The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period.PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation.This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Over Temperature Protection

A NTC resistor in series with a regular resistor should connect between RT and GND for emperature sensing and protection.NTC resistor value becomes lower when the ambient temperature rises.With the fixed internal current IRT flowing through the resistors,the voltage at RT pin becomes lower at high temperature.The internal OTP circuit is triggered and shutdown the MOSFET when the sensed input voltage is lower than VTH_OTP.

Gate Drive

2269-032 Gate is connected to the Gate of an external MOSFET for poweswitch control.Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI.

Good tradeoff is achieved through the built-in totem pole gate drive design with right output strength and dead time control.The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

Protection Controls

Good system reliability is achieved with 2269-032's rich protecti on features including Cycle- byCycle current limiting (OCP),Over Load Protection(OLP),over temperature protection(OTP), on chip VDD over voltage protection(OVP,optional)and under voltage lockout (UVLO).

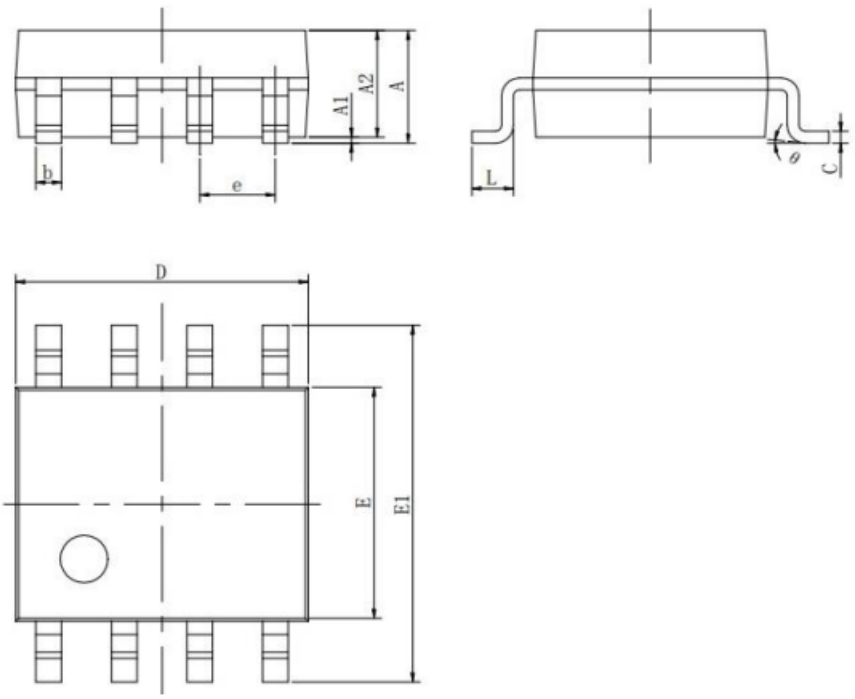
The OCP threshold value is self adjusted lower at higher current into VIN pin.This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage caused by inherent Over-Current sensing and control delay.A constant output power limit is achieved with recommended OCP compensation scheme on 2269-032.A toutput overload condition,FB voltage is biased higher.When FB input exceeds power limit threshold value for more than 80mS,control circuit reacts to turnoff the power MOSFET.

Similarly,control circuit shutdowns the power MOSFET when an Over Temperature condition is detected.2269-032 resumes the operation when temper ature drops below the hysteresis value.VDD 1S supplied with transformer auxiliary winding output.It is clamped when VDD is higher than 35V. MOSFET is shut down when VDD drops below UVLO(enter)limit and device enters power on startup sequence hereafter.

Outline Dimensions

SOP-8

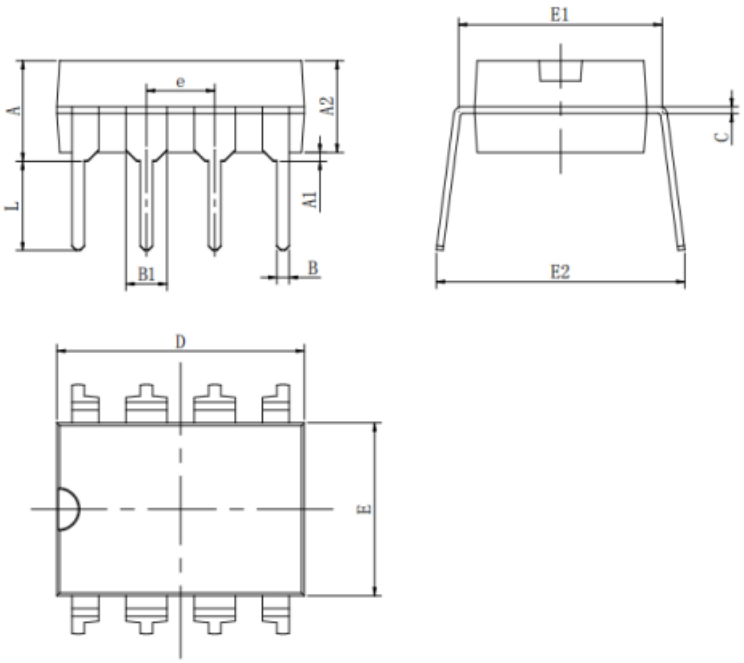
Unit : mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.800	0.053	0.071
A1	0.050	0.250	0.004	0.010
A2	1.250	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.170	0.250	0.006	0.010
D	4.780	5.000	0.185	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

DIP-8

Unit:mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

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