24C32

DATASHEET

Specification Revision History：

Version	Date	Description
V1.0	2019/03	New
V1.1	2021/12	Modify Ordering Information
V1.2	2025/02	Modify Ordering Information
V1.3	2025/03	Add application precautions and overall typesetting.

Two-Wire Serial EEPROM
16K(8-bit wide)

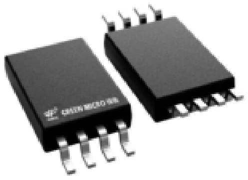
FEATURES

- Low voltage and low power operations:
    - 24C32: V_{CC} = 1.8V to 5.5V
- 32 bytes page write mode.
- Partial page write operation allowed.
- Internally organized: 4,096 × 8 (32K).
- Standard 2-wire bi-directional serial interface.
- Schmitt trigger, filtered inputs for noise protection.
- Self-timed Write Cycle (5ms maximum).
- 1000 kHz (2.5V-5V), 400 kHz (1.8V) Compatibility.
- Automatic erase before write operation.
- Write protect pin for hardware data protection.
- High reliability: typically 1,000,000 cycles endurance.
- 100 years data retention.
- Industrial temperature range (-40°C to 85°C).
- Standard 8-lead DIP/SOP/MSOP/TSSOP/DFN and 5-lead SOT23/TSOT23 packages

DESCRIPTION

The 24C32 series are 32,768 bits of serial Electrical Erasable and Programmable Read Only Memory, commonly known as EEPROM.They are organized as 4096 words of 8 bits(one byte)each.The devices are fabricated with proprietary advanced CMOS process for low power and low voltage applications. These devices are available in standard 8-lead DIP,8-lead SOP,8-lead MSOP,8-lead TSSOP,8-lead DFN,5-lead SOT23,and 5-lead TSOT23 packages.A standard 2-wire serial interface is used to address all read and write functions.Our extended Vcc range(1.8V to 5.5V)devices enables wide spectrum of applications.

The appearance of the product



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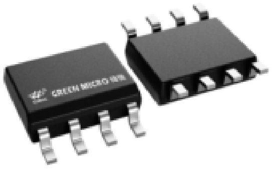
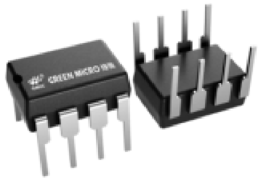


SOP-8



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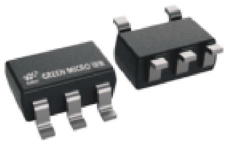

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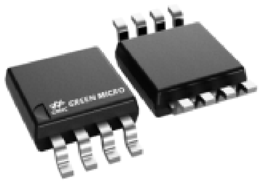


MSOP-8

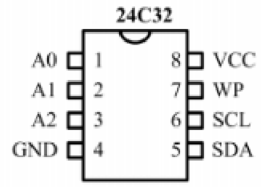
Ordering Information

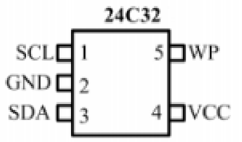
Product Model	Package Type	Marking	Packing	Packing Qty
AT24C32ACP(GMIC)	DIP-8	24C32 745	TUBE	2000PCS/BOX
AT24C32ACDR(GMIC)	SOP-8	24C32 745	REEL	4000PCS/REEL
AT24C32ACT(GMIC)	TSSOP-8	24C32 745	REEL	3000PCS/REEL
AT24C32ACS5(GMIC)	SOT23-5	24C32 745	REEL	3000PCS/REEL
AT24C32ACF(GMIC)	DFN-8(3x3)	24C32 745	REEL	5000PCS/REEL
AT24C32ACMDR(GMIC)	MSOP-8	24C32 745	REEL	3000PCS/REEL
GM24C32ACP	DIP-8	24C32 745	TUBE	2000PCS/BOX
GM24C32ACDR	SOP-8	24C32 745	REEL	4000PCS/REEL
GM24C32ACT	TSSOP-8	24C32 745	REEL	3000PCS/REEL
GM24C32ACS5	SOT23-5	24C32 745	REEL	3000PCS/REEL
GM24C32ACF	DFN-8(3x3)	24C32 745	REEL	5000PCS/REEL
GM24C32ACMDR	MSOP-8	24C32 745	REEL	3000PCS/REEL

PIN CONFIGURATION

Pin Name	Pin Function
A2,A1,A0	Device Address Inputs
SDA	Serial Data Input /Open Drain Output
SCL	Serial Clock Input
WP	Write Protect
NC	No-Connect
VCC	Power Supply
GND	Ground

All these packaging types come in conventional or Pb-free certified



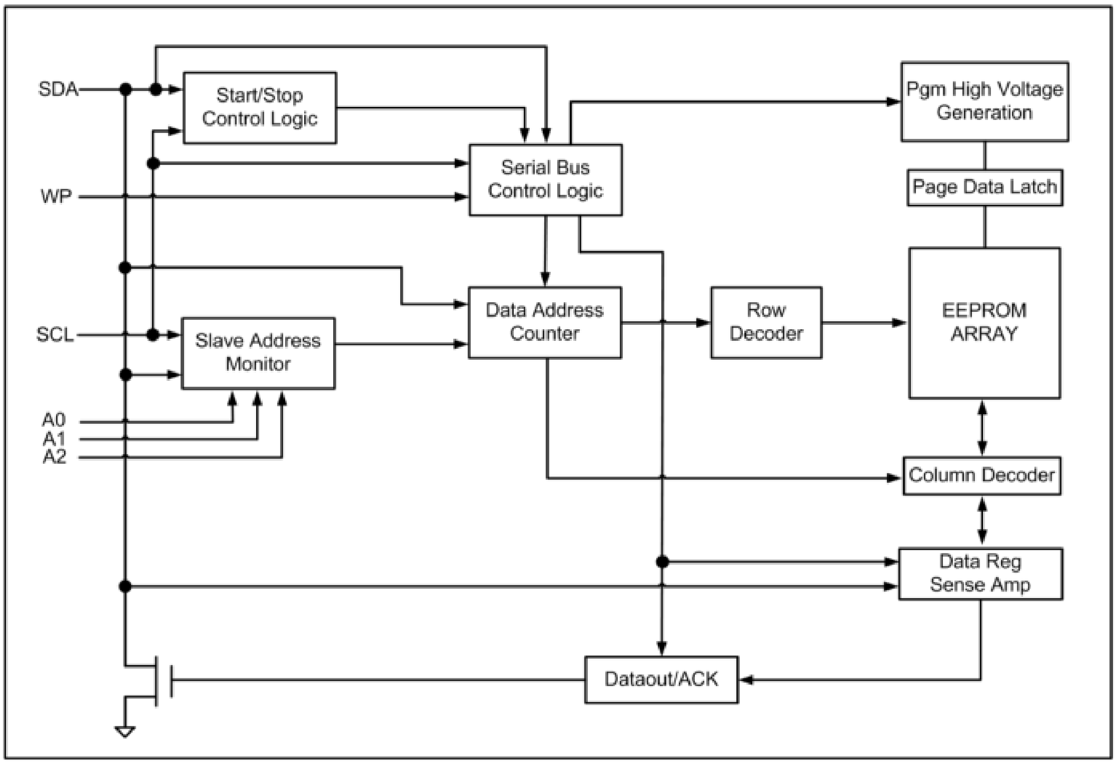


ABSOLUTE MAXIMUM RATINGS

Industrial operating temperature	-40℃ to 85℃
Storage temperature	-50℃ to 125℃
Input voltage on any pin relative to ground	0.3V to V_{CC}+0.3V
Maximum voltage	8V
ESD protection on all pins	>2000V

**Stresses exceed those listed under "Absolute Maximum Rating" may cause permanent damage to the device.Functional operation of the device at conditions beyond those listed in the specification is not guaranteed.Prolonged exposure to extreme conditions may affect device reliability or functionality.*

Block Diagram



Block Diagram

(A)SERIAL CLOCK (SCL)

The rising edge of this SCL input is to latch data into the EEPROM device while the falling edge of this clock is to clock data out of the EEPROM device.

(B)DEVICE/CHIP SELECT ADDRESSES (A2,A1,A0)

These are the chip select input signals for the serial EEPROM devices.Typically,these signals are hardwired to either VIH or Vn.If left unconnected,they are internally recognized as VL.However,due to capacitive coupling that may appear in customer applications,FMD recommends always connecting the address pins to a known state.When using a pull-up or pull-down resistor,FMD recommends using 10kΩ or less.

(C)SERIAL DATALINE(SDA)

SDA data line is a bi-directional signal for the serial devices.It is an open drain output signal and can be wired-OR with other open-drain output devices.

(D)WRITE PROTECT (WP)

The 24C32 devices have a WP pin to protect the whole EEPROM array from programming. Programming operations are allowed if WP pin is left un-connected or input to V_{IL}.Conversely all programming functions are disabled if WP pin is connected to V_{IH} or V_{CC}.Read operations is not affected by the WP pin's input level.If left unconnected,it is internally recognized as V_{IL}.However,due to capacitive coupling that may appear in customer applications,FMD recommends always connecting the WP pin to a known state.When using a pull-up or pull-down resistor,FMD recommends using 10kΩ or less.

MEMORY ORGANIZATION

The 24C32 devices have 128 pages respectively. Since each page has 32 bytes,random word addressing to 24C32 will require 12 bits data word addresses respectively.

DEVICE OPERATION

(A)SERIAL CLOCK AND DATA TRANSITIONS

The SDA pin is typically pulled to high by an external resistor.Data is allowed to change only when Serial clock SCL is at VIL.Any SDA signal transition may interpret as either a START or STOP condition as described below.

(B)START CONDITION

With SCL VIH,a SDA transition from high to low is interpreted as a START condition.All valid commands must begin with a START condition.

(C)STOP CONDITION

With SCL VIH,a SDA transition from low to high is interpreted as a STOP condition.All valid read or write commands end with a STOP condition.The device goes into the STANDBY mode if it is after a read command.A STOP condition after page or byte write command will trigger the chip into the STANDBY mode after the self-timed internal programming finish (see Figure 1).

(D)ACKNOWLEDGE

The 2-wire protocol transmits address and data to and from the EEPROM in 8 bit words.The EEPROM acknowledges the data or address by outputting a "0"after receiving each word.The ACKNOWLEDGE signal occurs on the 9th serial clock after each word.

(E)STANDBY MODE

The EEPROM goes into low power STANDBY mode after a fresh power up,after receiving a STOP bit in read mode,or after completing a self-time internal programming operation.

(F)SOFT RESET

After an interruption in protocol power loss or system reset,any two-wire part can be reset by following these steps:

1.Creat a START condition, 2.Clock eighteen data bits “1”,
3.Creat a start condition as SDA is high.

Figure 1: Timing diagram for START and STOP conditions

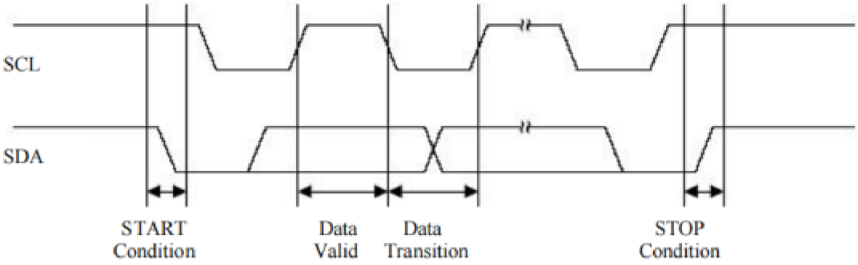
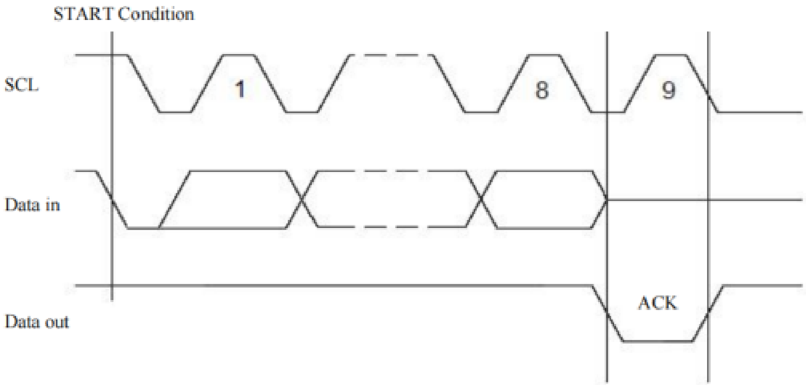


Figure 2: Timing diagram for output ACKNOWLEDGE



DEVICE ADDRESSING

The 2-wire serial bus protocol mandates an 8 bits device address word after a START bit condition to invoke a valid read or write command.The first four most significant bits of the device address must be 1010,which is common to all serial EEPROM devices.The next three bits are device address bits.These three otherwise the chip will go into STANDBY mode.However,matching may not be needed for some or all evice address bits (5th,6th and 7th)as noted below.The last or 8th bit is a read/write command bit.If the 8th bit is at VIH then the chip goes into read mode.If a "0" is detected,the device enters programming mode.

WRITE OPERATIONS

(A)BYTE WRITE

A write operation requires two 8-bit data word address following the device address word and ACKNOWLEDGE signal.Upon receipt of this address,the EEPROM will respond with a "0" and then clock in the first 8-bit data word.Following receipt of the 8-bit data word,the EEPROM will again output a "0" .The addressing device,such as a microcontroller,must terminate the write sequence with a STOP condition.At this time the EEPROM enters into an internally-timed write cycle state.All inputs are disabled during this write cycle and the EEPROM will not respond until the writing is completed (figure 3).

(B)PAGE WRITE

The 32K EEPROM are capable of 32-byte page write.

A page write is initiated the same way as a byte write,but the microcontroller does not send a STOP condition after the first data word is clocked in.The microcontroller can transmit up to 31 more data words after the EEPROM acknowledges receipt of the first data word.The EEPROM will respond with a "0" after each data word is received.The microcontroller must terminate the page write sequence with a STOP condition(see Figure 4).

The lower five bits of the data word address are internally incremented following the receipt of each data word.The higher data word address bits are not incremented,retaining the memory page row location. If more than 32 data words are transmitted to the EEPROM,the data word address will “roll over” and the previous data will be overwritten.

(C)ACKNOWLEDGE POLLING

ACKNOWLEDGE polling may be used to poll the programming status during a self-timed internal programming.By issuing a valid read or write address command,the EEPROM will not acknowledge at the 9th clock cycle if the device is still in the self-timed programming mode.However,if the programming completes and the chip has returned to the STANDBY mode,the device will return a valid ACKNOWLEDGE signal at the gth clock cycle.

READ OPERATIONS

The read command is similar to the write command except the 8t readwrite bit in address word is set to “1”. The three read operation modes are described as follows:

(A)CURRENT ADDRESS READ

The EEPROM internal address word counter maintains the last read or write address plus one if the power supply to the device has not been cut off.To initiate a current address read operation,the micro- controller issues a START bit and a valid device address word with the read/write bit(8th)set to “1”.The EEPROM will response with an ACKNOWLEDGE signal on the gth serial clock cycle.An 8-bit data word willthen be serially clocked out.The internal address word counter willthen automatically increase by one.For current address read the micro-controller will not issue an ACKNOWLEDGE signal on the 18th clock cycle.The micro-controller issues a valid STOP bit after the 18th clock cycle to terminate the read operation.The device then returns to STANDBY mode (see Figure 5).

(B)SEQUENTIAL READ

The sequential read is very similar to current address read.The micro-controller issues a START bit and a valid device address word with read/write bit(8th)set to “1”.The EEPROM will response with an ACKNOWLEDGE signal on the 9th serial clock cycle.An 8-bit data word will then be serially clocked out. Meanwhile the internally address word counter will then automatically increase by one.

Unlike current address read,the micro-controller sends an ACKNOWLEDGE signal on the 18th clock cycle signaling the EEPROM device that it wants another byte of data. Upon receiving the ACKNOWLEDGE signal,the EEPROM will serially clocked out an 8-bit data word based on the incremented internal address counter. If the micro-controller needs another data,it sends out an ACKNOWLEDGE signal on the 27th clock cycle.Another 8-bit data word will then be serially clocked out.This sequential read continues as long as the micro-controller sends an ACKNOWLEDGE signal after receiving a new data word.When the internal address counter reaches its maximum valid address, it rolls over to the beginning of the memory array address.Similar to current address read,the micro- controller can terminate the sequential read by not acknowledging the last data word received,but sending a STOP bit afterwards instead (figure 6).

(C)RANDOM READ

Random read is a two-steps process.The first step is to initialize the internal address counter with a target read address using a "dummy write"instruction.The second step is a current address read.

To initialize the internal address counter with a target read address,the micro-controller issues a START bit first,follows by a valid device address with the read/write bit(8th)set to “0”.The EEPROM will then acknowledge. The micro-controller will then send two address words. Again the EEPROM will acknowledge.Instead of sending a valid written data to the EEPROM,the micro-controller performs a current address read instruction to read the data.Note that once a START bit is issued,the EEPROM will reset the internal programming process and continue to execute the new instruction -which is to read the current address (figure 7).

Figure 3: Byte Write

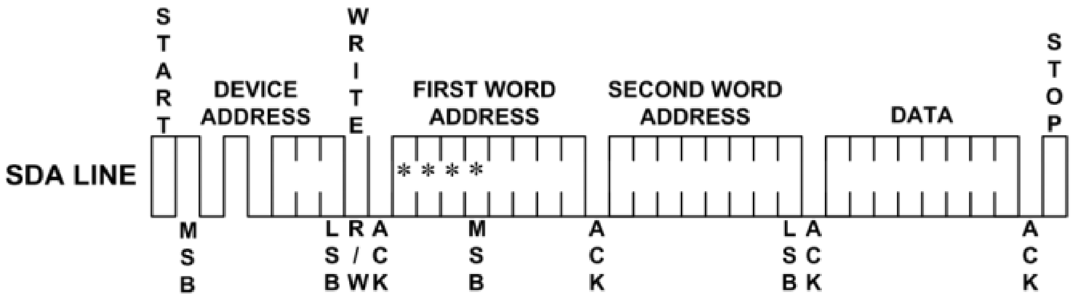


Figure 4: Page Write

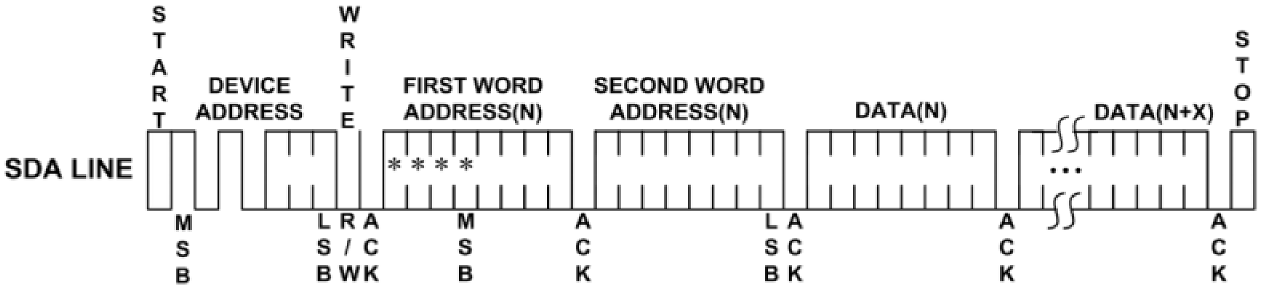


Figure 5: Current Address Read

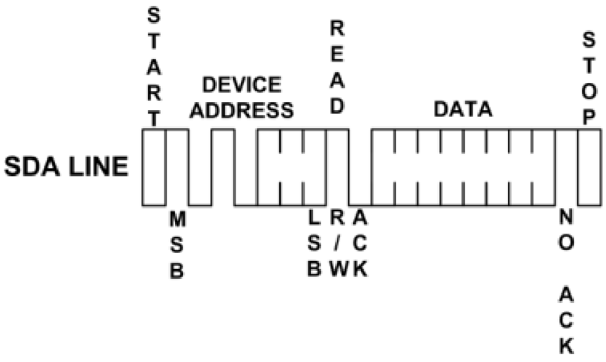


Figure 6: Sequential Read

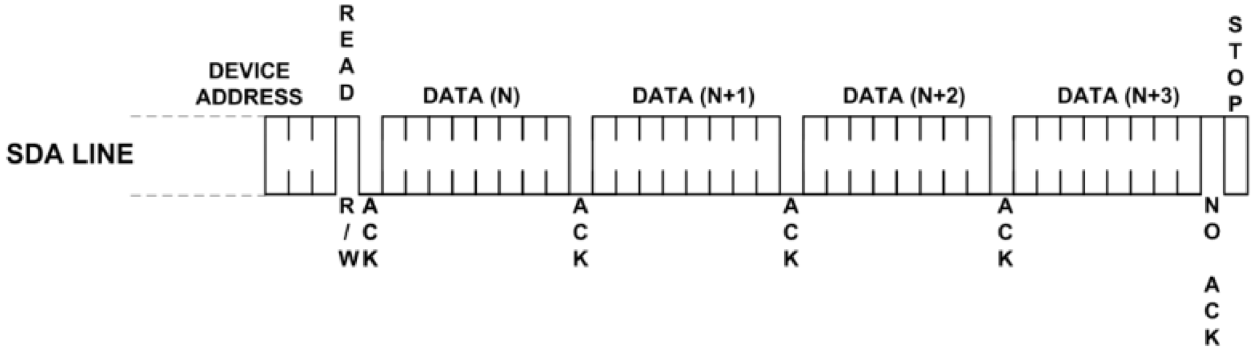
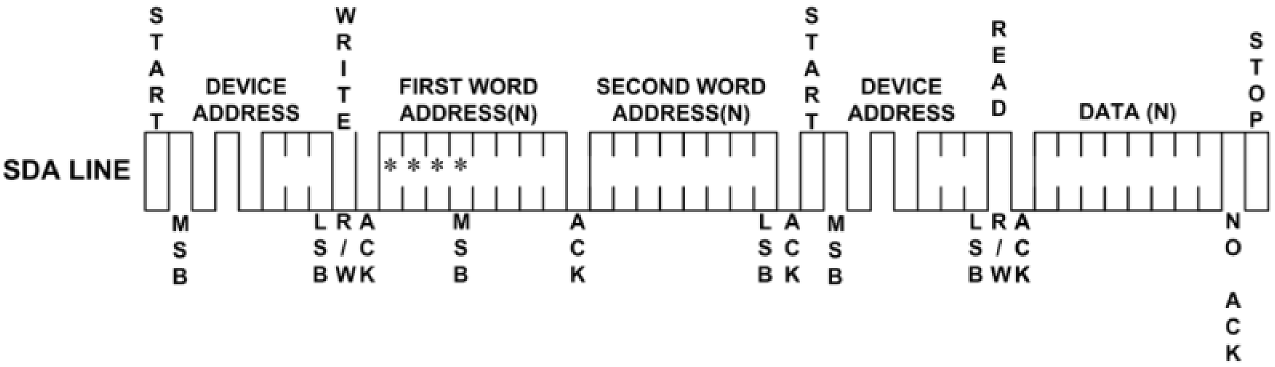
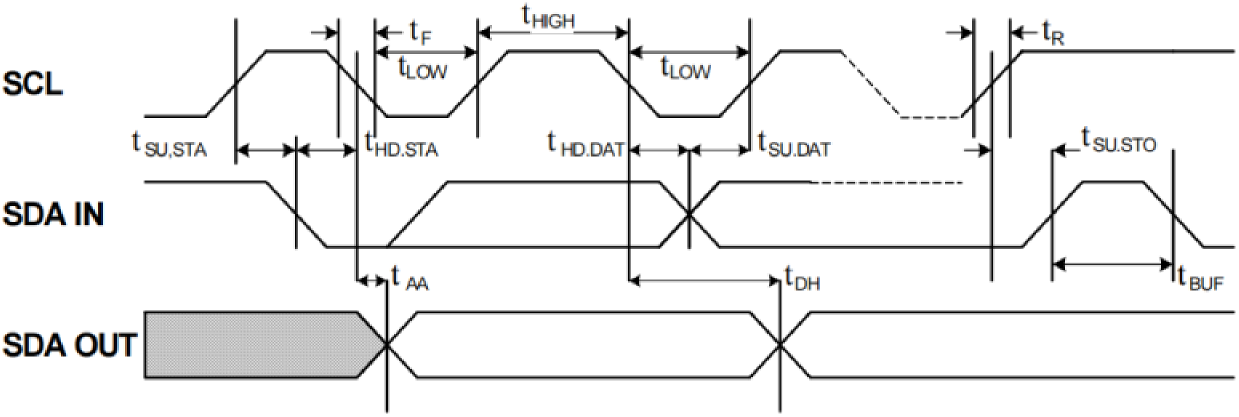


Figure 7: Random Read



Notes: 1) * = Don't Care bits

Figure 8: SCL and SDA Bus Timing



Electrical Specifications

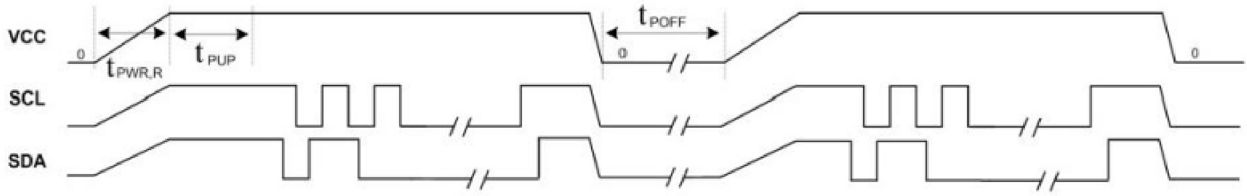
(A)Power-Up Requirements

During a power-up sequence,the VCC supplied to the device should monotonically rise from GND to the minimum VCC level,with a slew rate no faster than 0.05 V/µs and no slower then 0.1 V/ms.A decoupling cap should be connected to the VCC PAD which is no smaller than 10nF.

(B)Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence,this device includes a Power-on Reset(POR)circuit.Upon power-up,the device will not respond to any commands until the VCC level crosses the internal voltage threshold (V_{POR})that brings the device out of Reset and into Standby mode.The system designer must ensure the instructions are not sent to the device until the VCC supply has reached a stable value greater than or equal to the minimum VCC level.

Figure 9:Power on and Power down



If an event occurs in the system where the VCC level supplied to the device drops below the maximum VPOR level specified,it is recommended that a full power cycle sequence be performed by first driving the VCC pin to GND,waiting at least the minimum tpoFF time and then performing a new power-up sequence in compliance with the requirements defined in this section.

AC CHARACTERISTICS

Symbol	Parameter	1.8V		2.5V-5.5V		Unit
		Min	Max	Min	Max	
f_{SCL}	Clock frequency,SCL		400		1000	kHz
t_{LOW}	Clock pulse width low	1.3		0.4		µs
t_{HIGH}	Clock pulse width high	0.6		0.4		µs
t_{I}	Noise suppression time(1)		50		50	ns
t_{AA}	Clock low to data out valid	0.2	0.9	0.2	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1.3		0.5		µs
$t_{HD.STA}$	START hold time	0.6		0.25		µs
$t_{SU.STA}$	START set-up time	0.6		0.25		µs
$t_{HD.DAT}$	Data in hold time	0		0		µs
$t_{SU.DAT}$	Data in set-up time	100		100		ns
t_{R}	Input rise time(1)		300		300	ns
t_{F}	Input fall time(1)		300		300	ns
$t_{SU.STO}$	STOP set-up time	0.6		0.25		µs
t_{DH}	Date out hold time	50		50		ns
$t_{PWR.R}$(1)	Vcc slew rate at power up	0.1	50	0.1	50	V/ms
t_{PUP}(1)	Time required after VCC is stable before the device can accept commands	100		100		µs
t_{POFF}(1)	Minimum time at Vcc=0V between power cycles	500		500		ms
t_{WR}	Write cycle time		5		5	ms
Endurance(1)	25°C,Page Mode,3.3V	1,000,000				Write Cycles

Notes:

1.This Parameter is expected by characterization but are not fully screened by test.

2.AC Measurement conditions:

RL(Connects to Vcc):1.3KΩ

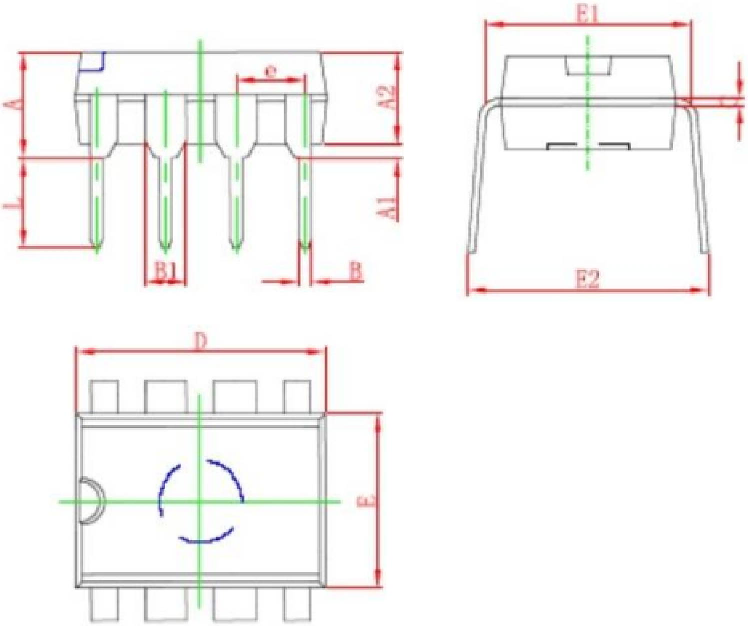
Input Pulse Voltages:0.3Vcc to 0.7V_{cc}

Input and output timing reference Voltages:0.5V_{cc}

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typical	Max	Units
V_{CC1}	24C××A supply V_{CC}		1.8		5.5	V
I_{CC1}	Supply read current	V_{CC}@5.0V SCL=400 kHz		0.4	1.0	mA
I_{CC2}	Supply write current	V_{CC}@5.0V SCL=400 kHz		2.0	3.0	mA
I_{SB1}	Supply current	V_{CC}@1.8V,V_{IN}=V_{CC} or Vss		<1.0		μA
I_{SB2}	Supply current	V_{CC} @2.5V,V_{IN}=V_{CC} or Vss		<1.0		μA
I_{SB3}	Supply current	V_{CC}@5.0V,V_{IN}=V_{CC} or Vss		<1.0		μA
I_{IL}	Input leakage current	VIn=V_{CC} or V_{SS}			3.0	μA
I_{LO}	Output leakage current	VIn=V_{CC} or V_{SS}			3.0	μA
V_{IL}	Input low level		-0.6		V_{CC}×0.3	V
V_{IH}	Input high level		V_{CC}×0.7		V_{CC}+0.5	V
V_{OL2}	Output low level	V_{CC} @3.0V,I_{OL}=2.1 mA			0.4	V
V_{OL1}	Output low level	V_{CC}@1.8V,I_{OL}=0.15 mA			0.2	V

DIP8 PACKAGE OUTLINE DIMENSIONS

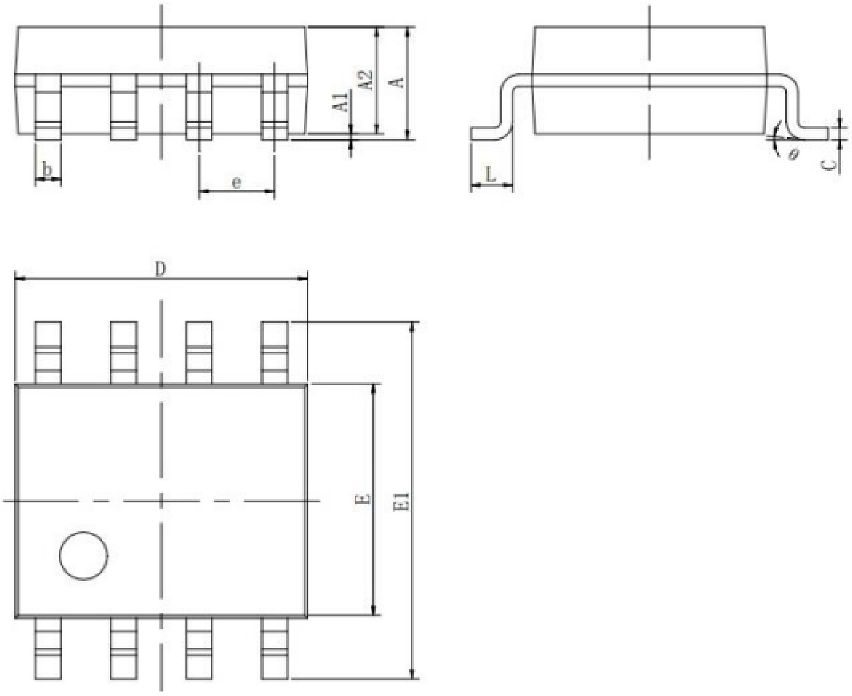


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540((BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

Outline Dimensions

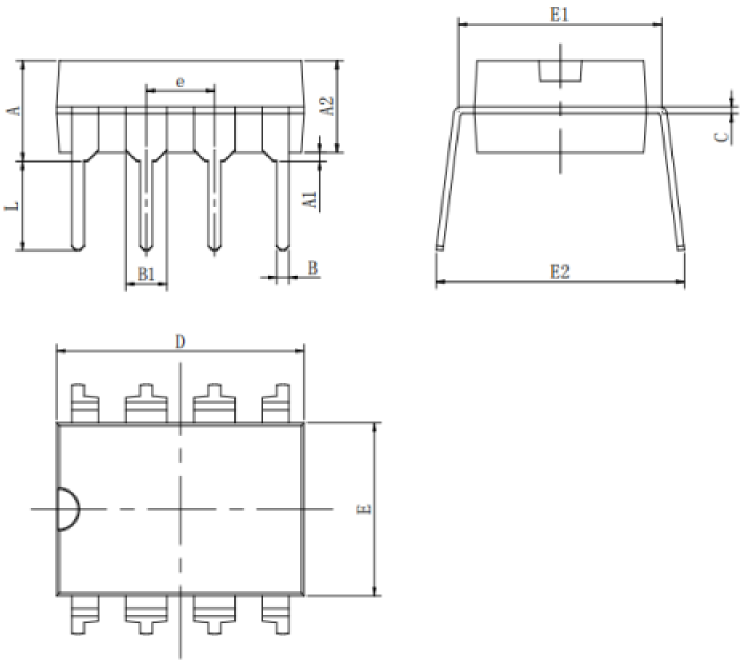
SOP-8

Unit : mm



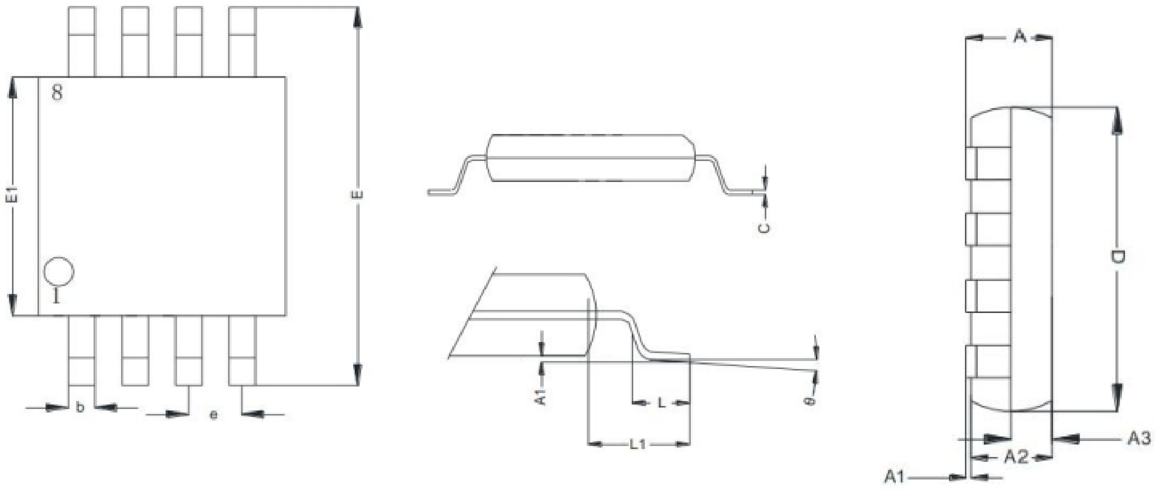
Symbol	DimensionsInMillimeters		DimensionsInInches	
	Min	Max	Min	Max
A	1.350	1.800	0.053	0.071
A1	0.050	0.250	0.004	0.010
A2	1.250	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.170	0.250	0.006	0.010
D	4.780	5.000	0.185	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

DIP-8 Unit:mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

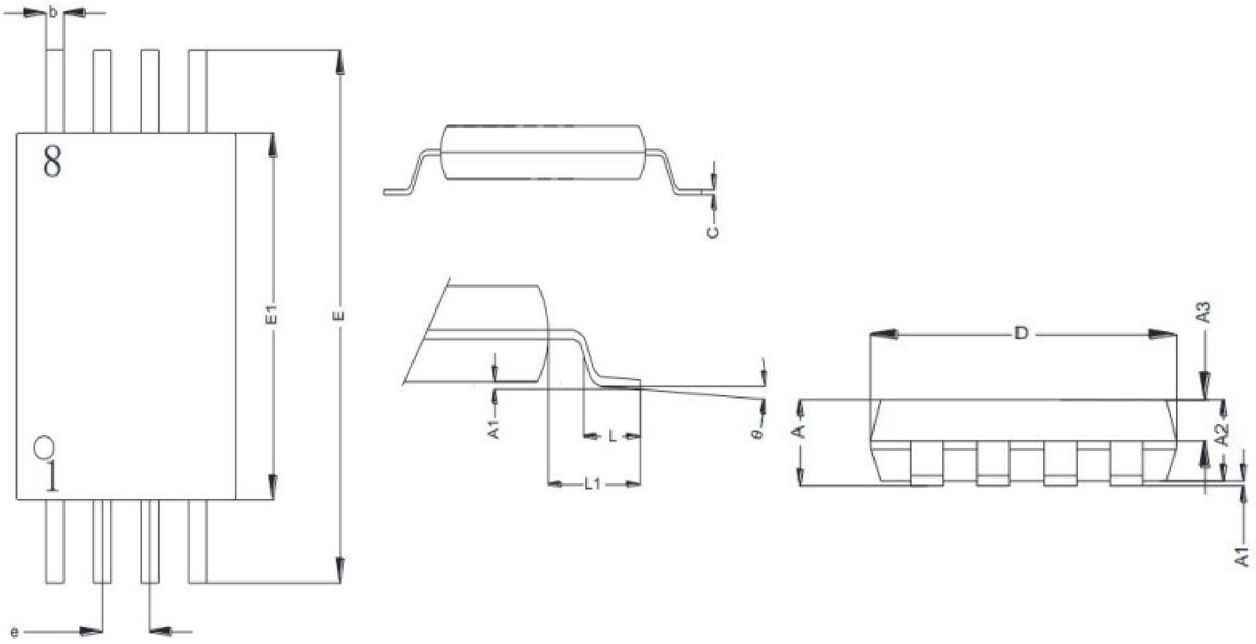
MSOP-8 Unit : mm



Symbol	Min	Typ	Max
A			1.100
A1	0.050		0.150
A2	0.750	0.850	0.950
A3	0.300	0.350	0.400
b	0.280		0.360
C	0.150		0.190
D	2.900	3.000	3.100
E	4.700	4.900	5.100
E1	2.900	3.000	3.100
e	-	0650	
L	0.400		0.700
L1		0.950	
θ	0		8°

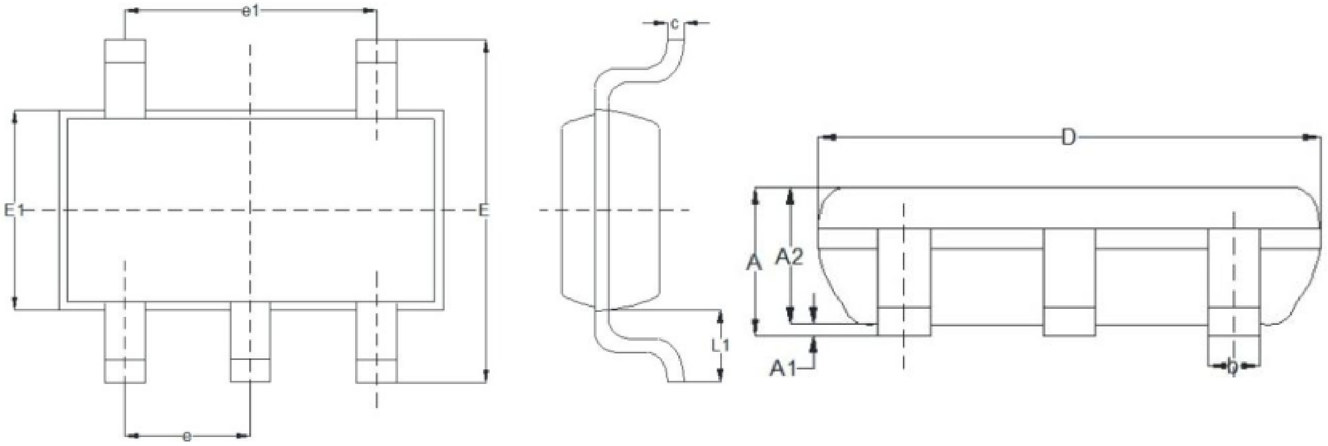
TSSOP-8

Unit : mm



Symbol	Min	Typ	Max
A			1.200
A1	0.050	-	0.150
A2	0.900		
A3	0.390	0.440	0.490
b	0.200		0.280
C	0.090		0.200
D	2.900	3.000	3.100
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e		0.650	
L	0.450	-	0.750
L1		1.000	-
θ	0		8°

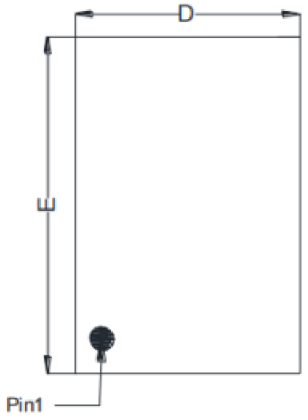
SOT23-5 Unit : mm



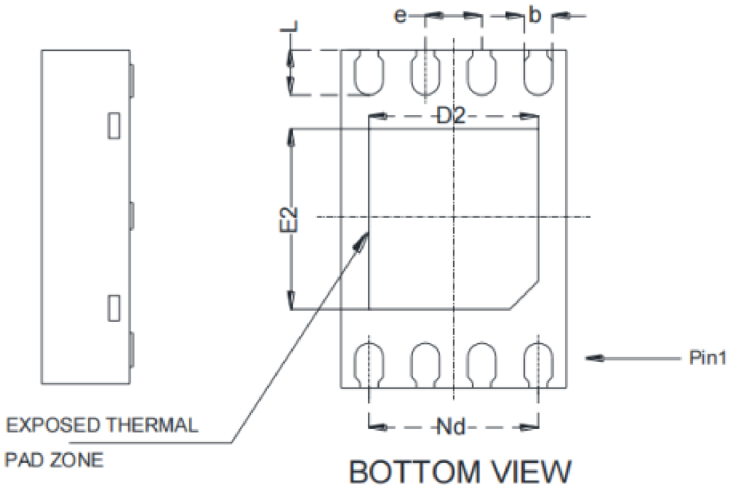
Symbol	Min	Typ	Max
A	1.000		1.250
A1	0.030		0.090
A2	1.050		1.150
c	0.080		0.200
D	2.900BSC		
E	2.800BSC		
E1	1.600BSC		
e	0.950BSC		
e1	1.900BSC		
L1	0.600REF		
b	0.300		0.450

DFN8(UN)

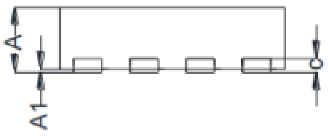
Unit：mm



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Min	Typ	Max
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
b	0.18	0.24	0.30
D	1.90	2.00	2.10
D2	1.30		1.60
E	2.90	3.00	3.10
E2	1.20		1.70
e		0.50	
L	0.25	-	0.50
c	0.10	0.15	0.20
Nd	-	1.50	

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