4606

DATASHEET

Specification Revision History:

Version	Date	Description
V1.0	2019/08	New
V1.1	2021/05	Modify Ordering Information
V1.2	2025/02	Modify Ordering Information
V1.3	2025/03	Add application precautions and overall typesetting.

N and P-Channel 30-V(D-S)MOSFET

GENERAL DESCRIPTION

The 4606 is the N and P Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery
loss are needed in a very small outline surface mount package.

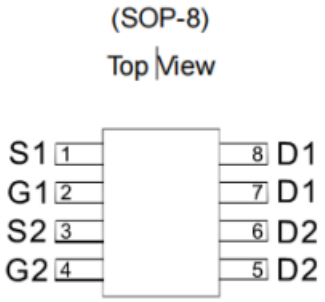
Features

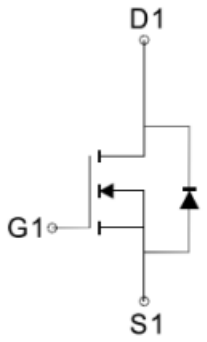
- $R_{DS}(ON) \leqslant 25m\Omega @ V_{GS}=10V$(N-Ch)
- $R_{DS}(ON) \leqslant 40m\Omega @ V_{GS}=4.5V$(N-Ch)
- $R_{DS}(ON) \leqslant 35m\Omega @ V_{GS}=-10V$(P-Ch)
- $R_{DS}(ON) \leqslant 58m\Omega @ V_{GS}=-4.5V$(P-Ch)
- Super high density cell design for extremely low RDS(ON)
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

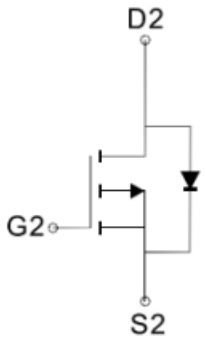
- Power Management
- DC/DC Converter
- LCD TV&Monitor Display inverter
- CCFL inverter
- LCD Display inverter

PIN CONFIGURATION





N-Channel MOSFET



P-Channel MOSFET

Ordering Information: 4606 (Pb-free)

Absolute Maximum Ratings (TA=25℃ Unless Otherwise Noted)

Parameter		Symbol	N-Channel Maximum Ratings	P-Channel Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A=25°C	I_D	7.1	-6	A
	T_A=70°C		5.7	-4.8	
Pulsed Drain Current		I_{DM}	28	-24	
Maximum Power Dissipation	T_A=25°C	P_D	2	2	W
	T_A=70°C		1.3	1.3	
Operating Junction Temperature		T_J	-55 to 150		°C
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	62.5	62.5	°C/W

*The device mounted on 1in2 FR4 board with 2 oz copper

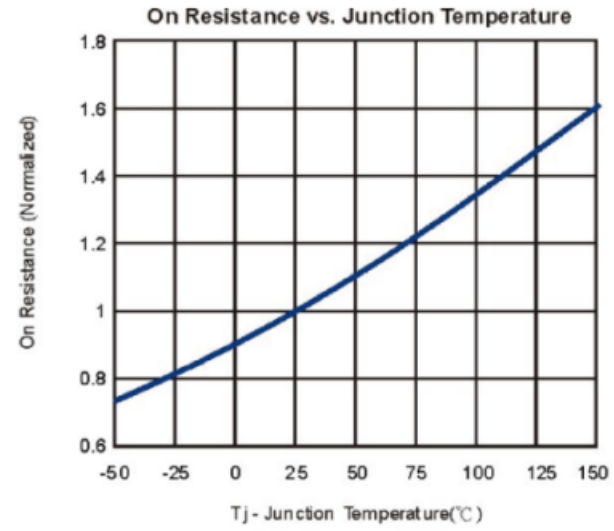
N and P-Channel 30-V(D-S)MOSFET

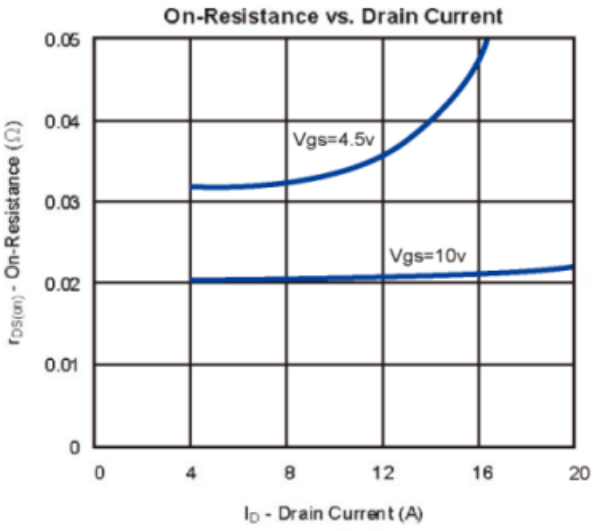
Electrical Characteristics(TA=25°C Unless Otherwise Specified)

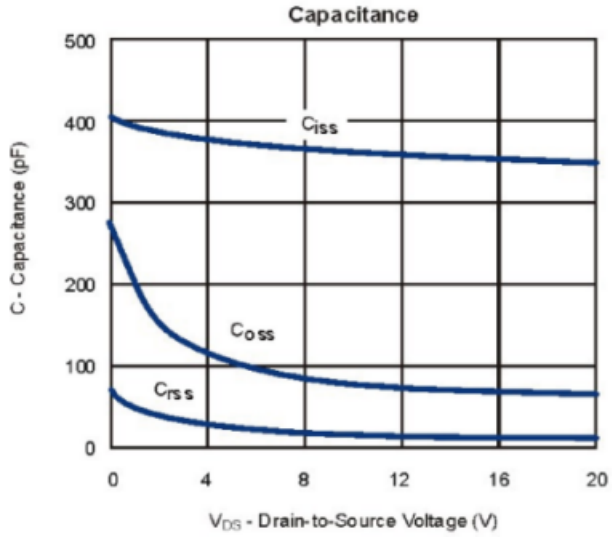
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
STATIC							
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=250μA V_{GS}=0V,I_D=-250μA	N-Ch P-Ch	30 -30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA V_{DS}=V_{GS},I_D=-250μA	N-Ch P-Ch	1.0 -1.0		3.0 -3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V,V_{GS}=±20V	N-Ch P-Ch			±100 ±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V,V_{GS}=0V V_{DS}=-30V,V_{GS}=0V	N-Ch P-Ch			1 -1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V,I_D=6.7A V_{GS}=-10V,I_D=-6.1A	N-Ch P-Ch		21 30	25 35	mΩ
		V_{GS}=4.5V,I_D=5.0A V_{GS}=-4.5V,I_D=-5.0A	N-Ch P-Ch		32 40	40 57	
V_{SD}	Diode Forward Voltage	Is=1.7A,V_{GS}=0V Is=-1.7A,V_{GS}=0V	N-Ch P-Ch		0.8 -0.8	1.2 -1.2	V
DYNAMIC							
Qg	Total Gate Charge	N-Channel V_{DS}=15V,V_{GS}=10V,I_D=6.7A P-Channel V_{DS}=-15V,V_{GS}=-10V,I_D=-6.1A	N-Ch P-Ch		12 21		nC
Qgs	Gate-Source Charge		N-Ch P-Ch		2 4		
Qgd	Gate-Drain Charge		N-Ch P-Ch		2.5 6		
Ciss	Input Capacitance	N-Channel V_{DS}=15V,V_{GS}=0V,f=1MHz P-Channel V_{DS}=15V,V_{GS}=0V,f=1MHz	N-Ch P-Ch		360 840		pF
Coss	Output Capacitance		N-Ch P-Ch		70 120		
Crss	Reverse Transfer Capacitance		N-Ch P-Ch		17 32		
Rg	Gate Resistance	Vos=0V,V_{GS}=0V,f=1MHz	N-Ch P-Ch		0.5 5.5		Ω
$t_{d(on)}$	Tum-On Delay Time	N-Channel V_{DD}=15V,RL=15Ω I_D=1A,VGEN=10V,Rg=6Ω P-Channel V_{DD}=-15V,R_L=15Ω I_D=-1A,VGEN=-10V,R_G=6Ω	N-Ch P-Ch		9.3 32		ns
t_r	Turn-On Rise Time		N-Ch P-Ch		14 13		
$t_{d(off)}$	Tum-Off Delay Time		N-Ch P-Ch		32 58		
t_f	Tum-Off FallTime		N-Ch P-Ch		3.2 6.8		

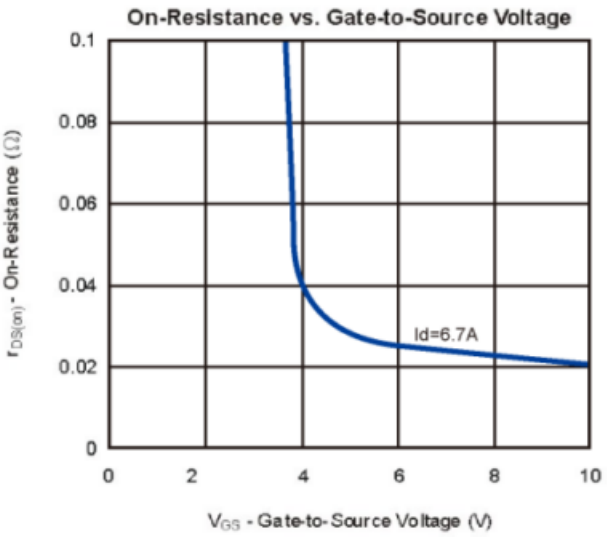
Notes:a.Pulse test;pulse width≤300us,duty cycle≤2%

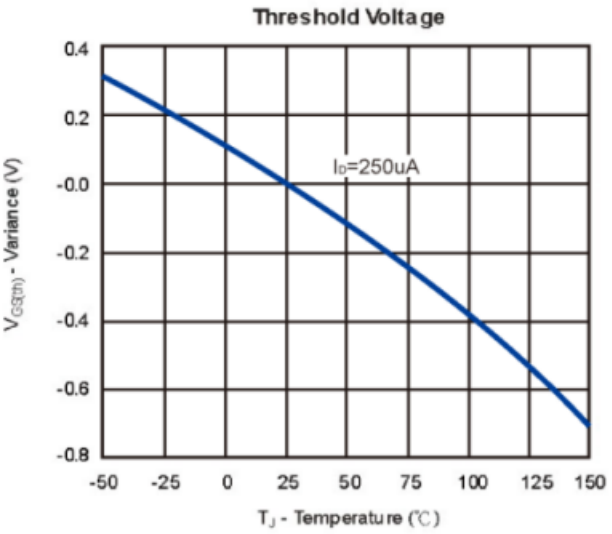
N and P-Channel 30-V(D-S)MOSFET Typical Characteristics(TJ=25°C Noted)

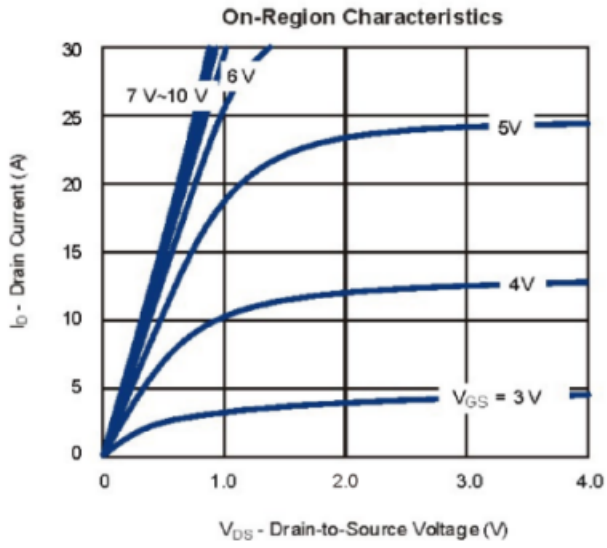








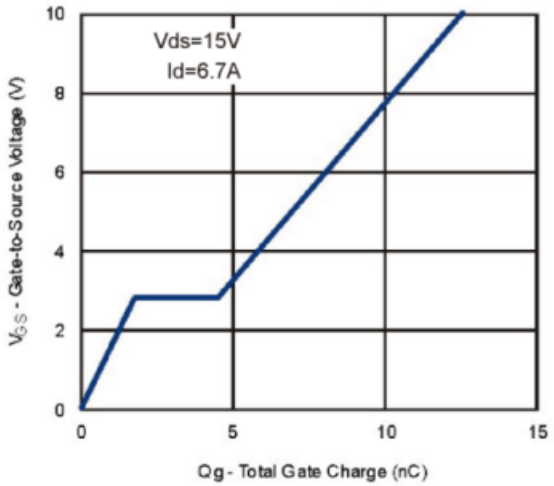




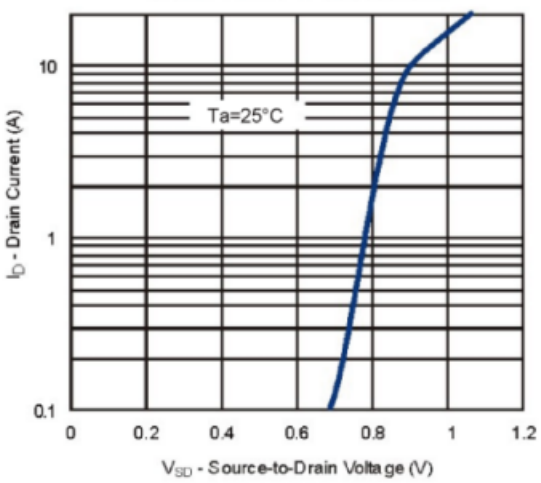
N and P- Channel 30-V (D-S) MOSFET04 ATypical Characteristics (TJ=25°C Noted)

N-CHANNEL

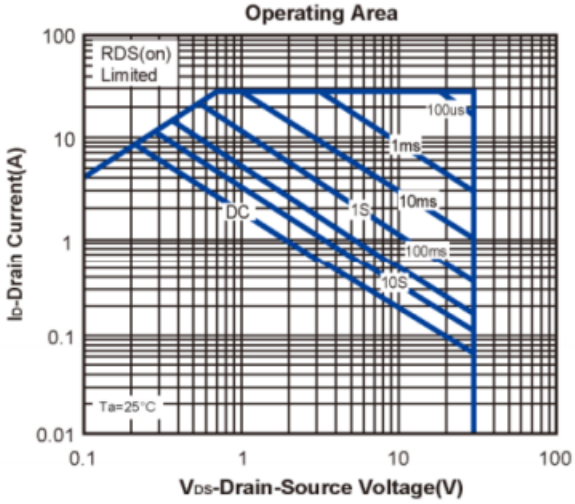
Gate Charge



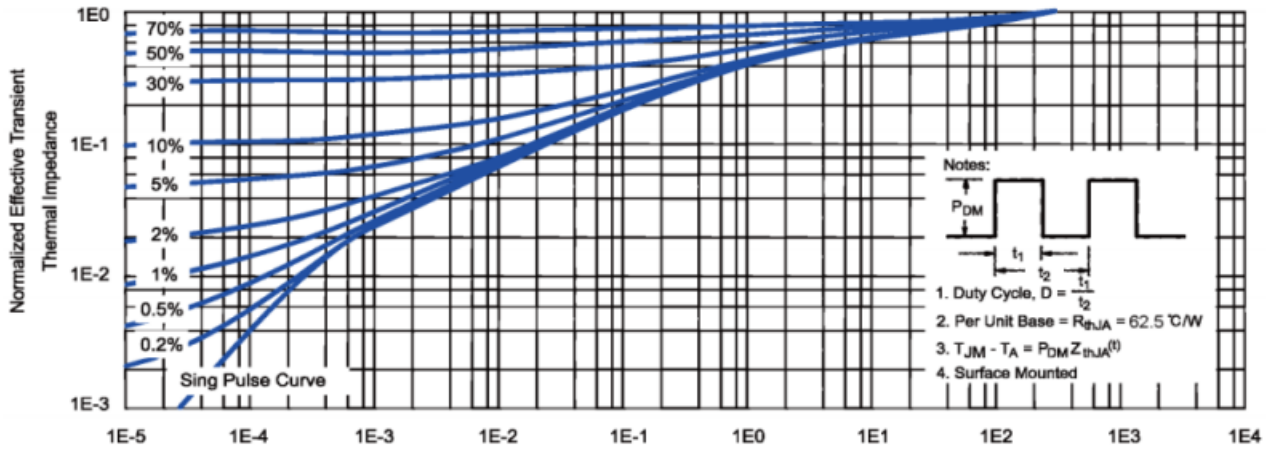
Body-diode characteristics



Maximum Forward Biased Safe Operating Area



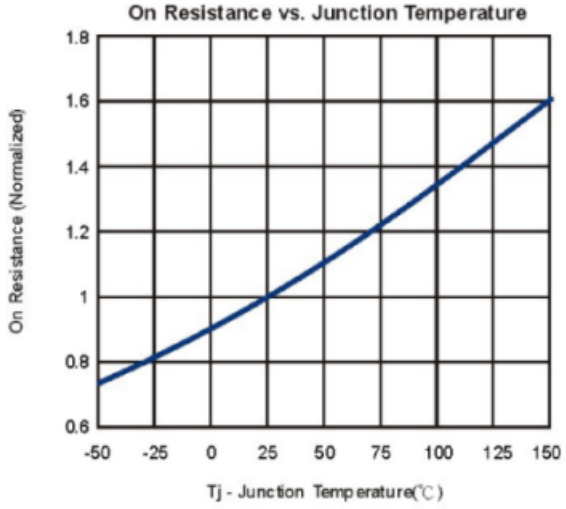
Normalized Thermal Transient Impedance, Junction-to-Ambient



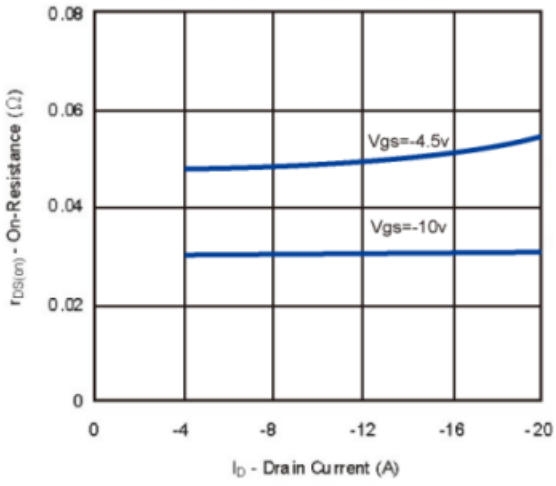
N and P-Channel 30-V(D-S)MOSFET Typical Characteristics(TJ=25°C Noted)

P-CHANNEL

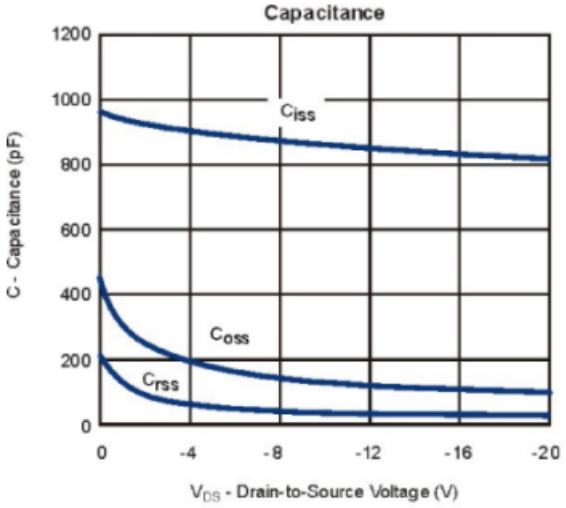
On Resistance vs. Junction Temperature



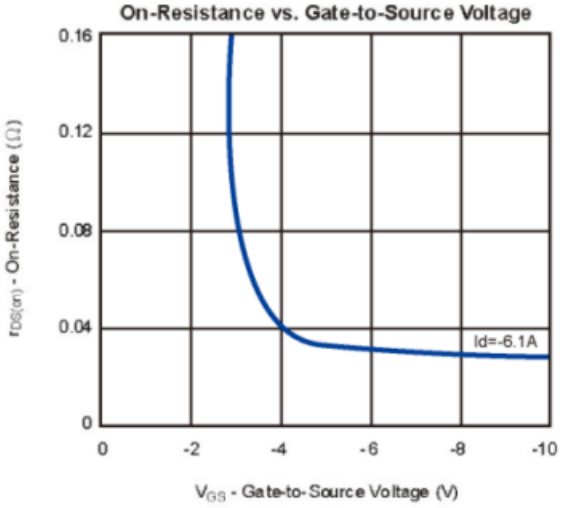
On-Resistance vs. Drain Current



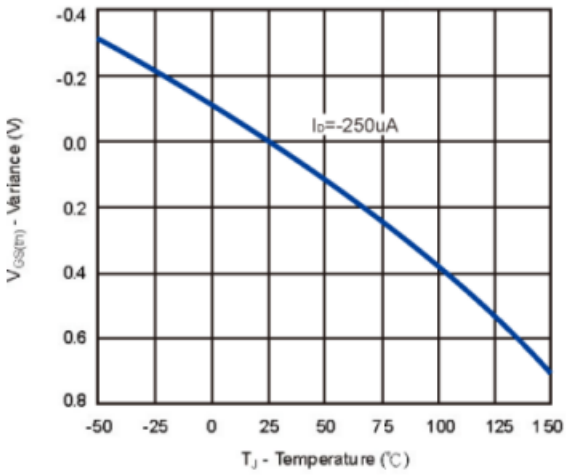
Capacitance



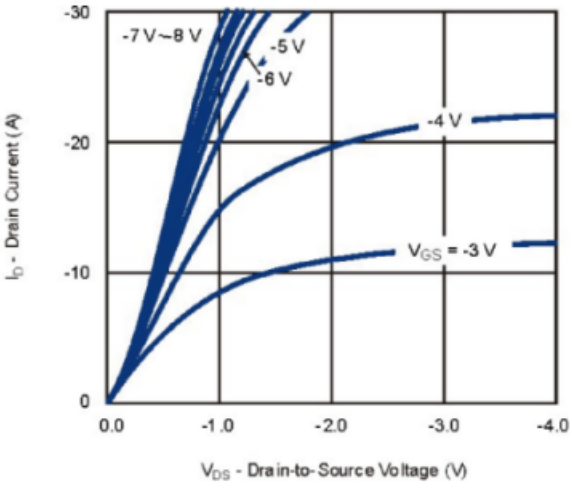
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

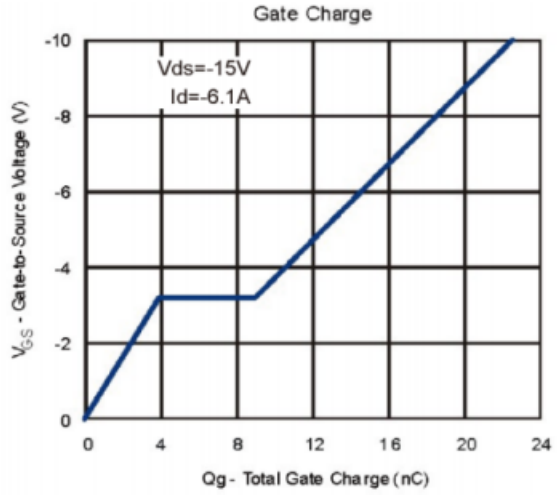


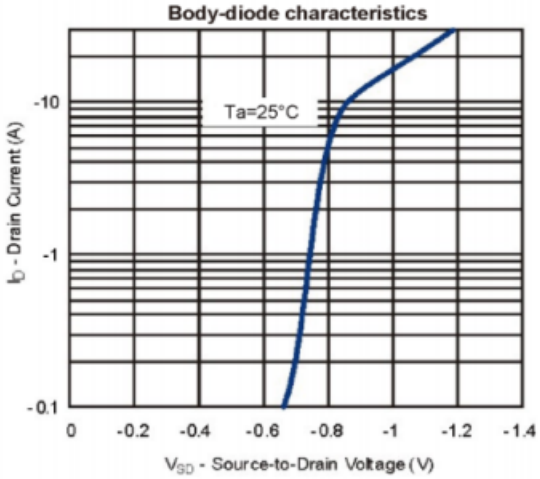
On-Region Characteristics

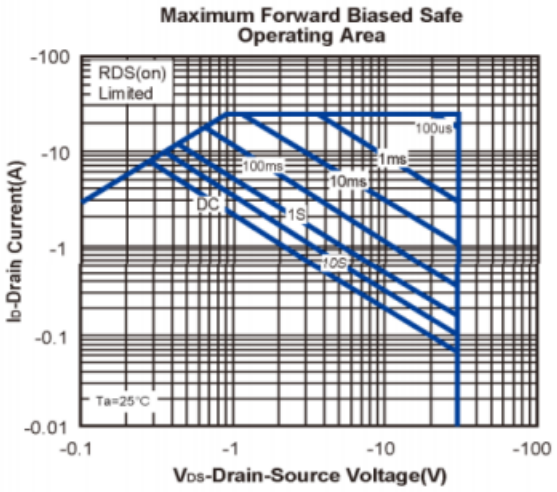


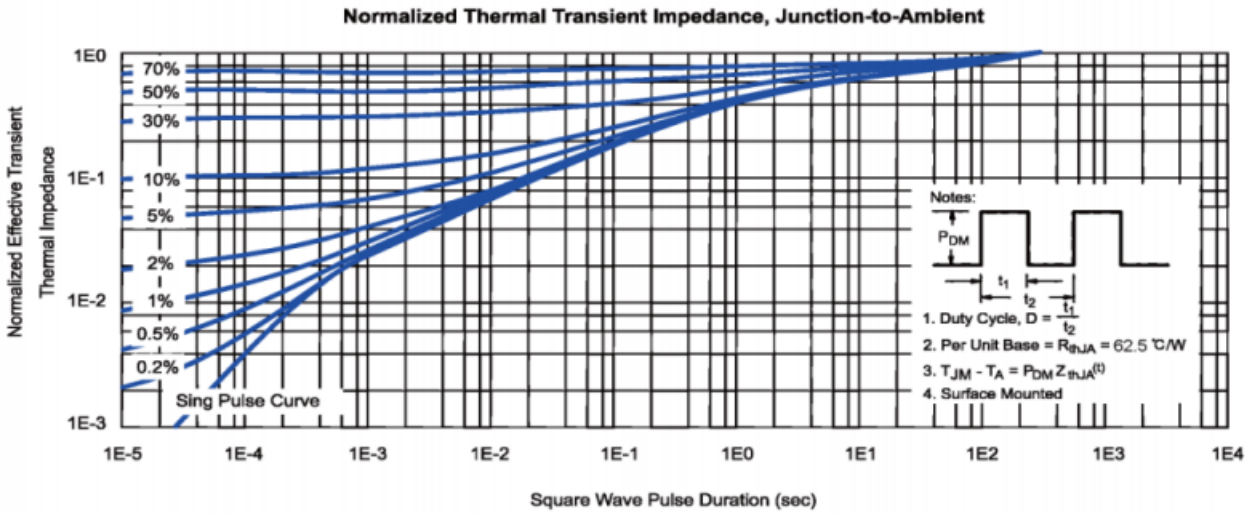
N and P-Channel 30-V(D-S)MOSFET Typical Characteristics(TJ=25°C Noted)

P-CHANNEL



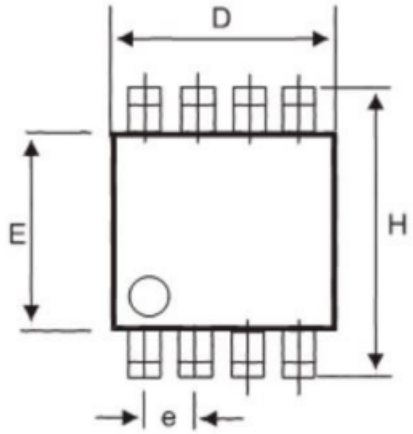


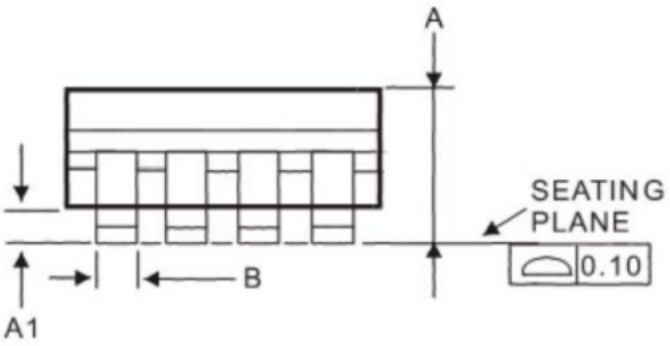


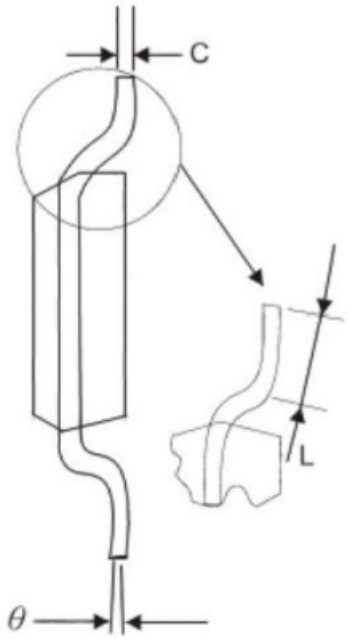


N and P-Channel 30-V(D-S)MOSFET

SOP-8 Package Outline







DIM	MILLIMETERS(mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note:1.Refer to JEDEC MS-012AA.

2.Dimension "D" does not include mold flash,protrusions or gate burrs.Mold flash,protrusions or gate burrs shall not exceed 0.15 mm per side.

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